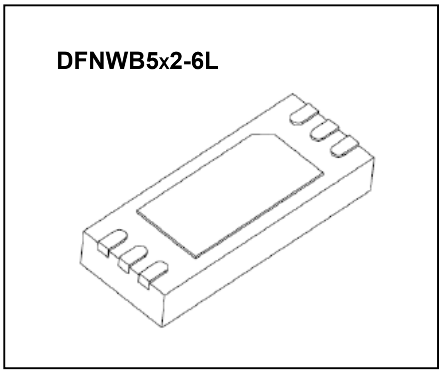
JSCJ

JIANGSU CHANGJING ELECTRONICS TECHNOLOGY CO., LTD.

DFNWB5×2-6L Plastic-Encapsulate MOSFETS

CJND2004S **Dual N-Channel MOSFET**

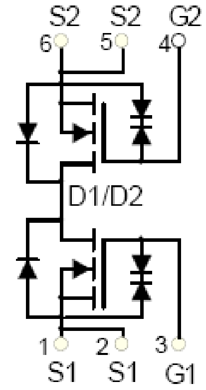
$V_{(BR)DSS}$	$R_{DS(on)}$TYP	I_D
18V	8.9 mΩ@4.5V	10A
	9.2 mΩ@4.0V	
	9.3 mΩ@3.8V	
	9.6 mΩ@3.1V	
	10.4 mΩ@2.5V	



DESCRIPTION

The CJND2004S uses advanced trench technology to provide excellent RDS(ON) and low gate charge. It is ESD protected. This device is suitable for use as a uni-directional or bi-directional load switch,facilitated by its common-drain configuration.

Equivalent Circuit



MARKING

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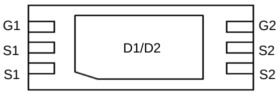

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MAXIMUM RATINGS (T_a=25℃ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	18	V
Gate-Source Voltage	V_{GS}	±12	V
Continuous Drain Current	I_D	10	A
Pulsed Drain Current	I_{DM} ①	40	A
Single Pulsed Avalanche Energy	E_{AS} ②	45	mJ
Power Dissipation	P_D	1.25	W
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$ ⑤	100	℃/W
Operating Junction and Storage Temperature Range	T_J ,T_{stg}	-55~+150	℃

MOSFET ELECTRICAL CHARACTERISTICS

T_a=25℃ unless otherwise specified

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Off characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =250μA	18			V
Zero gate voltage drain current	I_{DSS}	V_{DS} =16V, V_{GS} =0V			1.0	μA
Gate-body leakage current	I_{GSS}	V_{DS} =0V, V_{GS} =±4.5V			±1.0	μA
		V_{DS} =0V, V_{GS} =±8V			±10	μA
On characteristics ③						
Gate-threshold voltage	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =250μA	0.4	0.82	1.1	V
Static drain-source on-sate resistance	$R_{DS(on)}$	V_{GS} =4.5V, I_D =3A	6.4	8.9	11.6	mΩ
		V_{GS} =4.0V, I_D =3A	6.5	9.2	12.0	mΩ
		V_{GS} =3.8V, I_D =3A	6.6	9.3	12.1	mΩ
		V_{GS} =3.1V, I_D =3A	6.9	9.6	12.5	mΩ
		V_{GS} =2.5V, I_D =3A	7.4	10.4	13.5	mΩ
Dynamic characteristics ③④						
Input capacitance	C_{iss}	V_{DS} =10V,V_{GS} =0V, f =1MHz		1180		pF
Output capacitance	C_{oss}			176		
Reverse transfer capacitance	C_{rss}			141		
Gate resistance	R_g	f =1MHz		15		Ω
Switching characteristics ③④						
Total gate charge	Q_g	V_{GS}=4.5V, V_{DS}=10V, I_D=7A		12.3		nC
Gate-source charge	Q_{gs}			1.5		
Gate-drain charge	Q_{gd}			3.2		
Turn-on delay time	$t_{d(on)}$	VGS=4.5V,V_{DD}=10V, R_L=1.6Ω ,R_G=10Ω		2.4		ns
Turn-on rise time	t_r			6.7		
Turn-off delay time	$t_{d(off)}$			46		
Turn-off fall time	t_f			100		
Drain-Source Diode Characteristics						
Drain-source diode forward voltage	V_{SD} ③	V_{GS} =0V, I_S=5A			1.2	V
Continuous drain-source diode forward current	I_S				10	A
Pulsed drain-source diode forward current	I_{SM} ①				40	A

Notes:

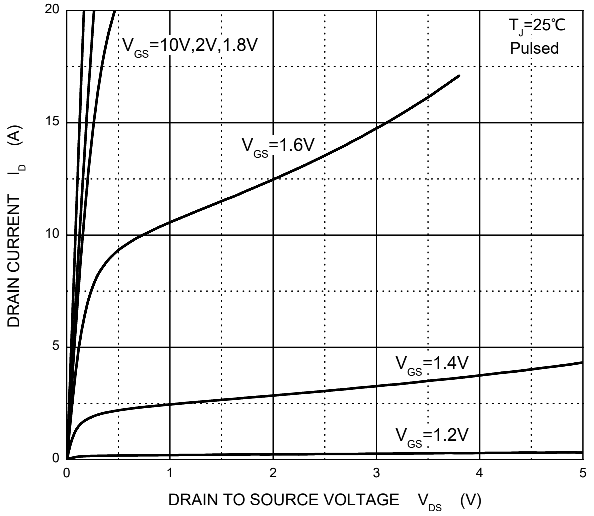
1.P_W≤10μs, Duty cycle≤1%.

2.EAS condition: V_{DD}=10V,V_{GS}=10V, L=0.5mH, Rg=25Ω Starting T_J= 25℃.

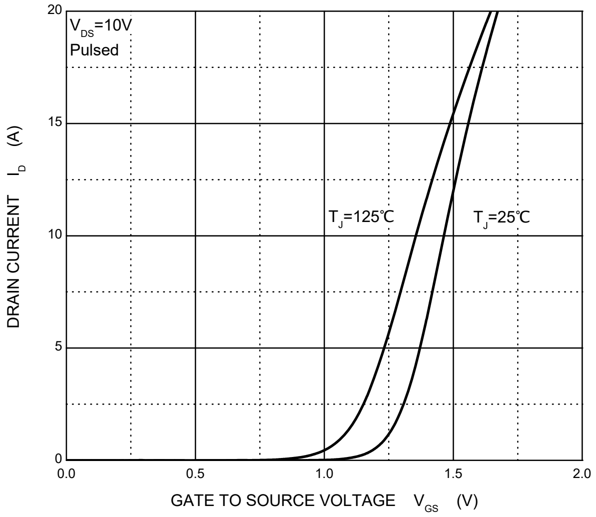
3.Pulse Test : Pulse Width≤300μs, duty cycle ≤2%.

4.Guaranteed by design, not subject to production.

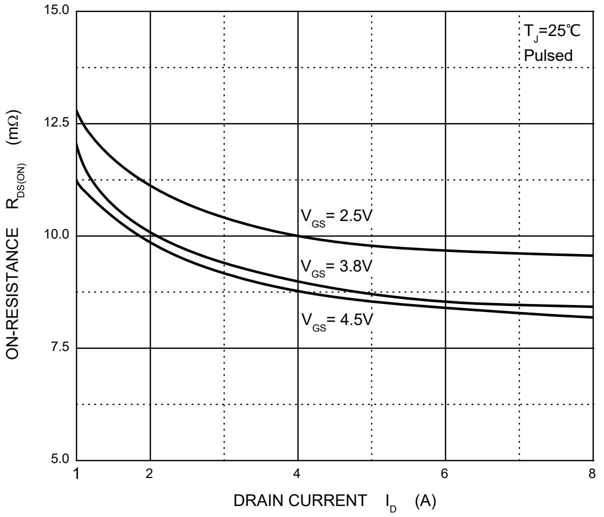
5.The value of $R_{\theta JA}$ is measured with one-side device actived mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_a=25℃.



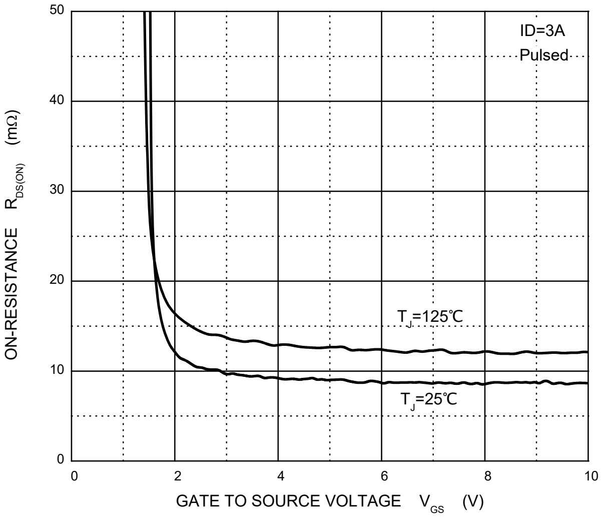
Output Characteristics



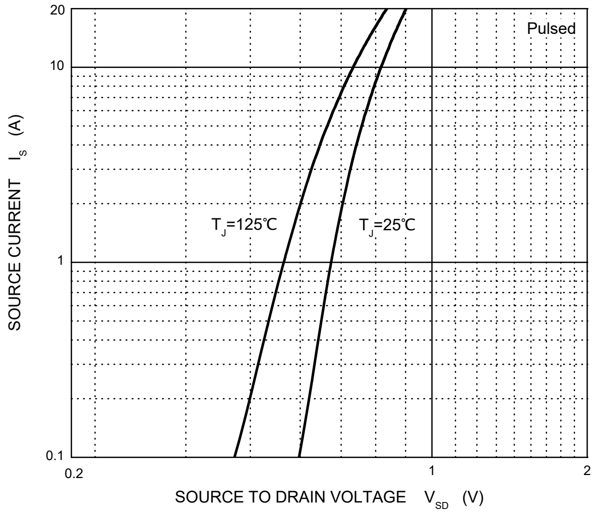
Transfer Characteristics



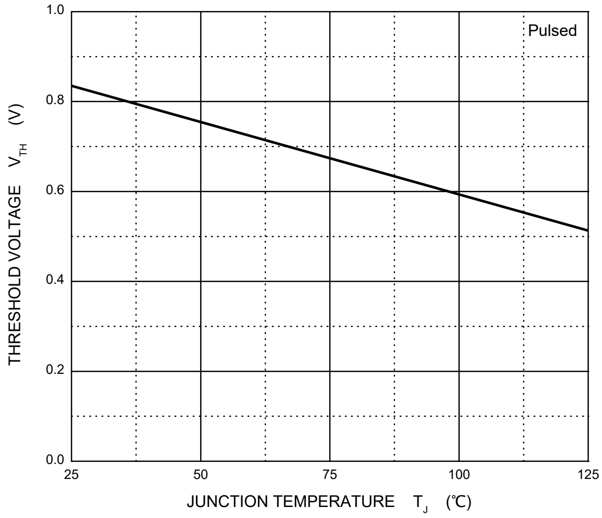
$R_{DS(ON)}$ —— I_D



$R_{DS(ON)}$ —— V_{GS}

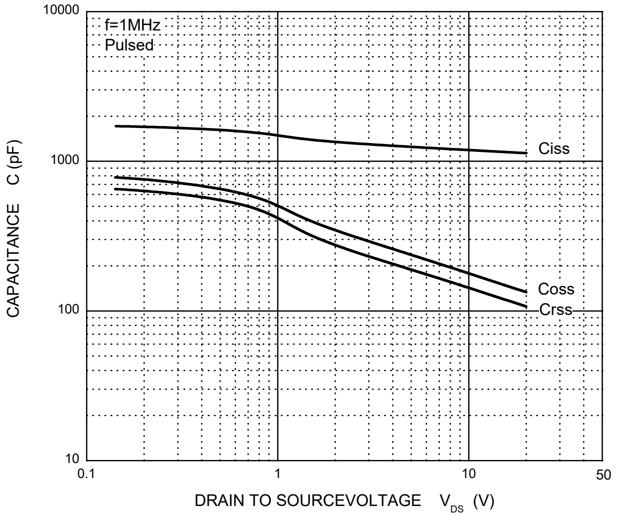


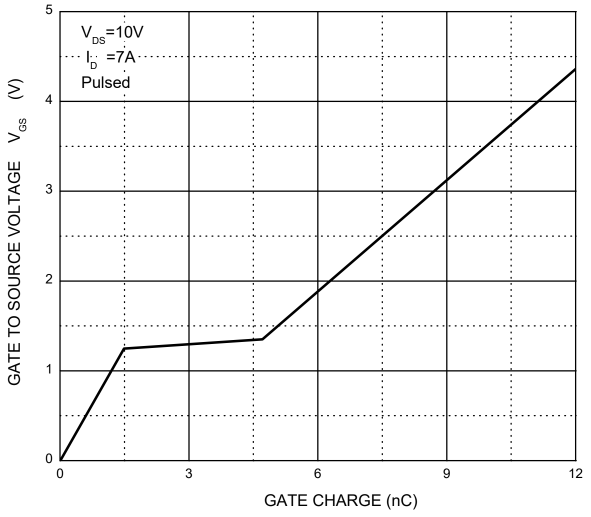
I_S —— V_{SD}

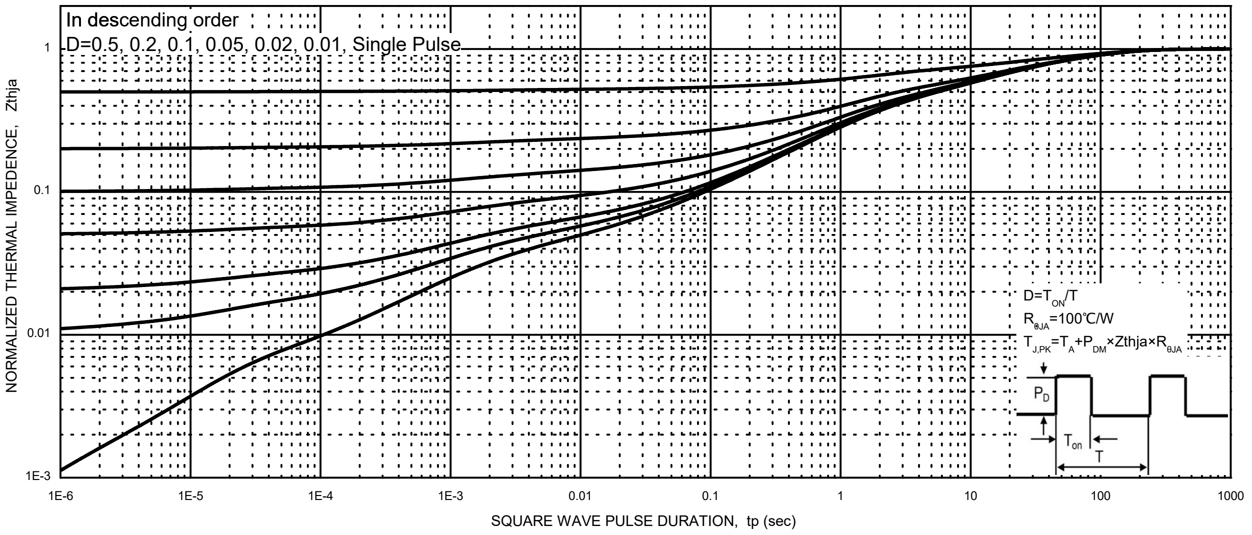


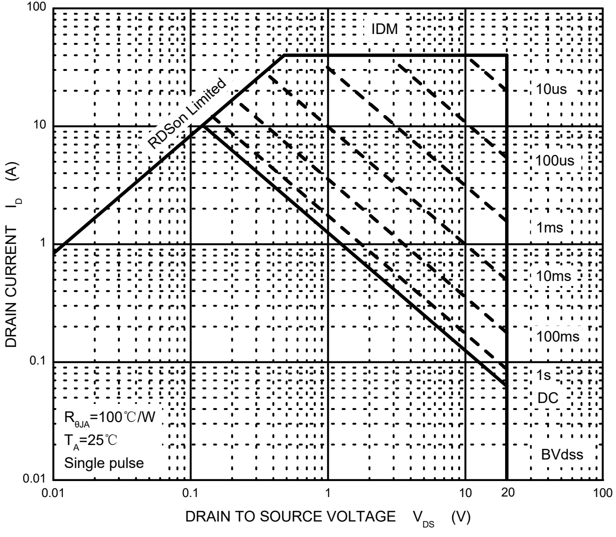
Threshold Voltage

Typical Characteristics

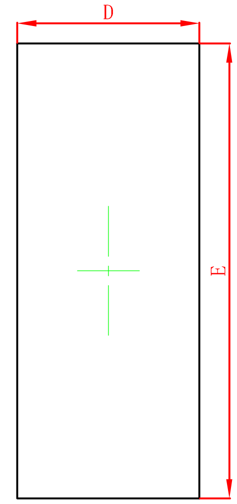

Capacitances


Gate Charge

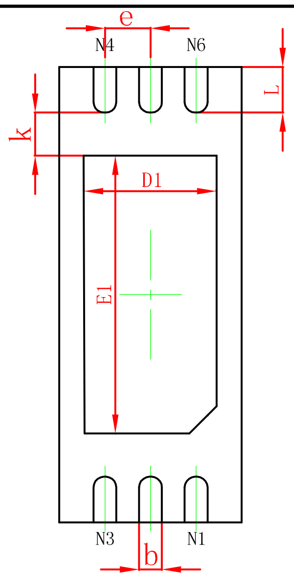

NORMALIZED TRAISIENT THERMAL IMPENDANCE


MAXIMUM FORWARD BIASED SAFE OPERATING AREA

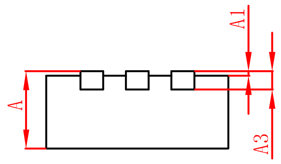
DFNWB5×2-6L-A Package Outline Dimensions(Unit:mm)



Top View



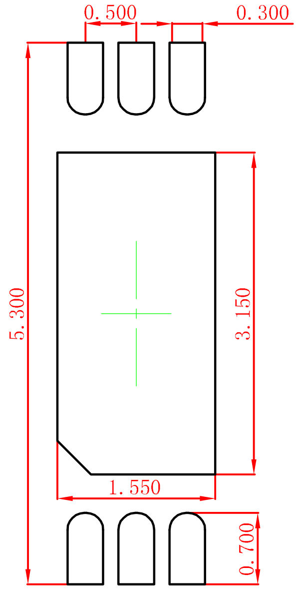
Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	1.924	2.076	0.076	0.082
E	4.924	5.076	0.194	0.200
D1	1.350	1.550	0.053	0.061
E1	2.950	3.150	0.116	0.124
k	0.200MIN.		0.008MIN.	
b	0.200	0.300	0.008	0.012
e	0.500TYP.		0.020TYP.	
L	0.424	0.576	0.017	0.023

DFNWB5×2-6L-A Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.050mm.
3.The pad layout is for reference purposes only.