X-Bit Bidirectional Level-Shifting, Voltage-Level Translator

CJTB010X Logic

1 Introduction

The CJTB010X is an 8-bit, dual supply translating transceiver with auto direction sensing, that enables bidirectional voltage level translation. It features two 8-bit input-output ports (An and Bn), one output enable input (OE) and two supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). $V_{CC(A)}$ can be supplied at any voltage between 1.2V and 3.6V and $V_{CC(B)}$ can be supplied at any voltage between 1.65V and 5.5V, making the device suitable for translating between any of the low voltage nodes (1.2V, 1.5V, 1.8V, 2.5V, 3.3V and 5.0 V).

Pins An and OE are referenced to $V_{CC(A)}$ and pins Bn are referenced to $V_{CC(B)}$. A LOW level at pin OE causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2 Available Packages

PART NUMBER	PACKAGE
CJTB0101	SOT-23-6L
	SOT-363
CJTB0102	TSSOP8(3x3)
	VSSOP8
CJTB0104	SOP14
	TSSOP14
	QFN3x2.5-14L
	QFN3.5x3.5-14L
CJTB0106	SOP16
	TSSOP16
CJTB0108	SOP20
	TSSOP20

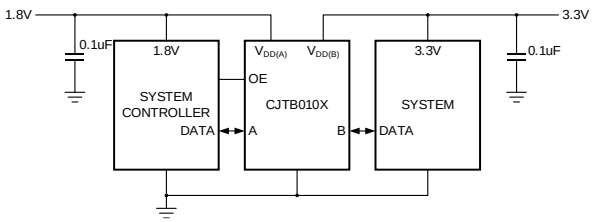
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Wide supply voltage range:
  - $V_{CC(A)}$: 1.2V to 3.6V
  - $V_{CC(B)}$: 1.65V to 5.5V
- I_{OFF} circuitry provides partial Power-down mode operation
- Inputs accept voltages up to 5.5V
- Specified from -40°C to +125°C

4 Applications

- Handsets
- Smartphones
- Tablets
- Desktop PCs



Typical operating circuit

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJTB0101M6N	SOT-23-6L	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 3000 Units/Reel	Active
CJTB0101R6N	SOT-363	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 3000 Units/Reel	Active
CJTB0102BAN	TSSOP8(3x3)	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 3000 Units/Reel	Active
CJTB0102VAN	VSSOP8	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 3000 Units/Reel	Active
CJTB0104ADN	SOP14	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units/Reel	Active
CJTB0104BDN	TSSOP14	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units/Reel	Active
CJTB0104QBN	QFN3x2.5-14L	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 3000 Units/Reel	Active
CJTB0104QIN	QFN3.5x3.5-14L	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units/Reel	Active
CJTB0106AEN	SOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units/Reel	Active
CJTB0106BEN	TSSOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units/Reel	Active
CJTB0108AGN	SOP20	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 2000 Units/Reel	Active
CJTB0108BGN	TSSOP20	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units/Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

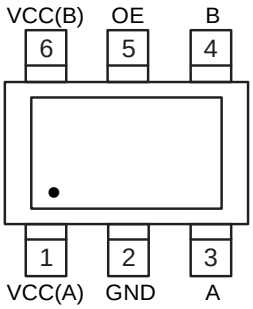
MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

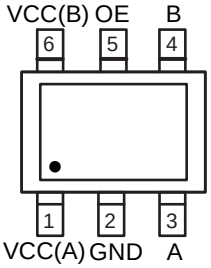
6 Pin Configuration and Marking Information

6.1 Pin Configuration

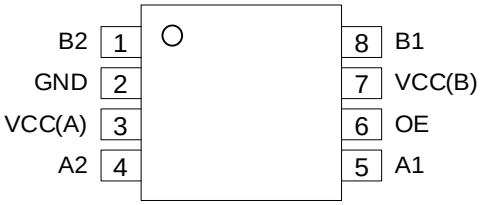
SOT-23-6L



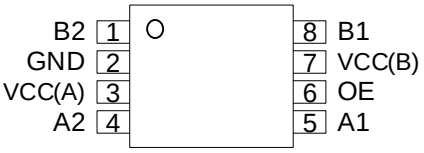
SOT-363



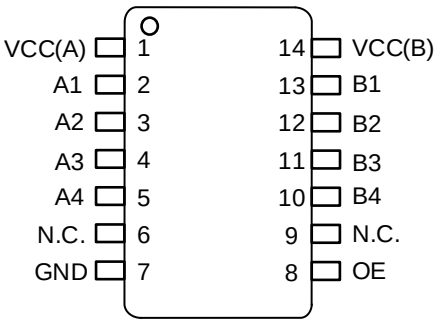
TSSOP8(3x3)



VSSOP8



SOP14



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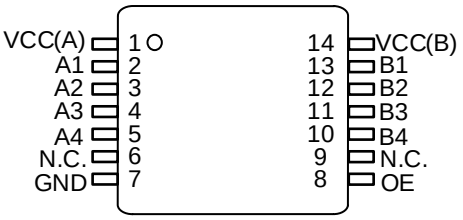
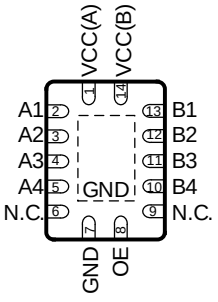


QFN3x2.5-14L



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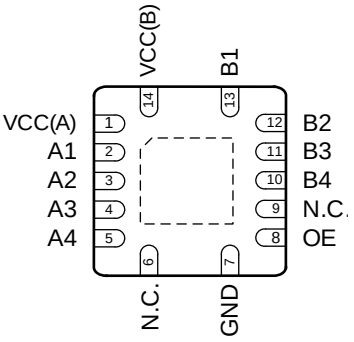


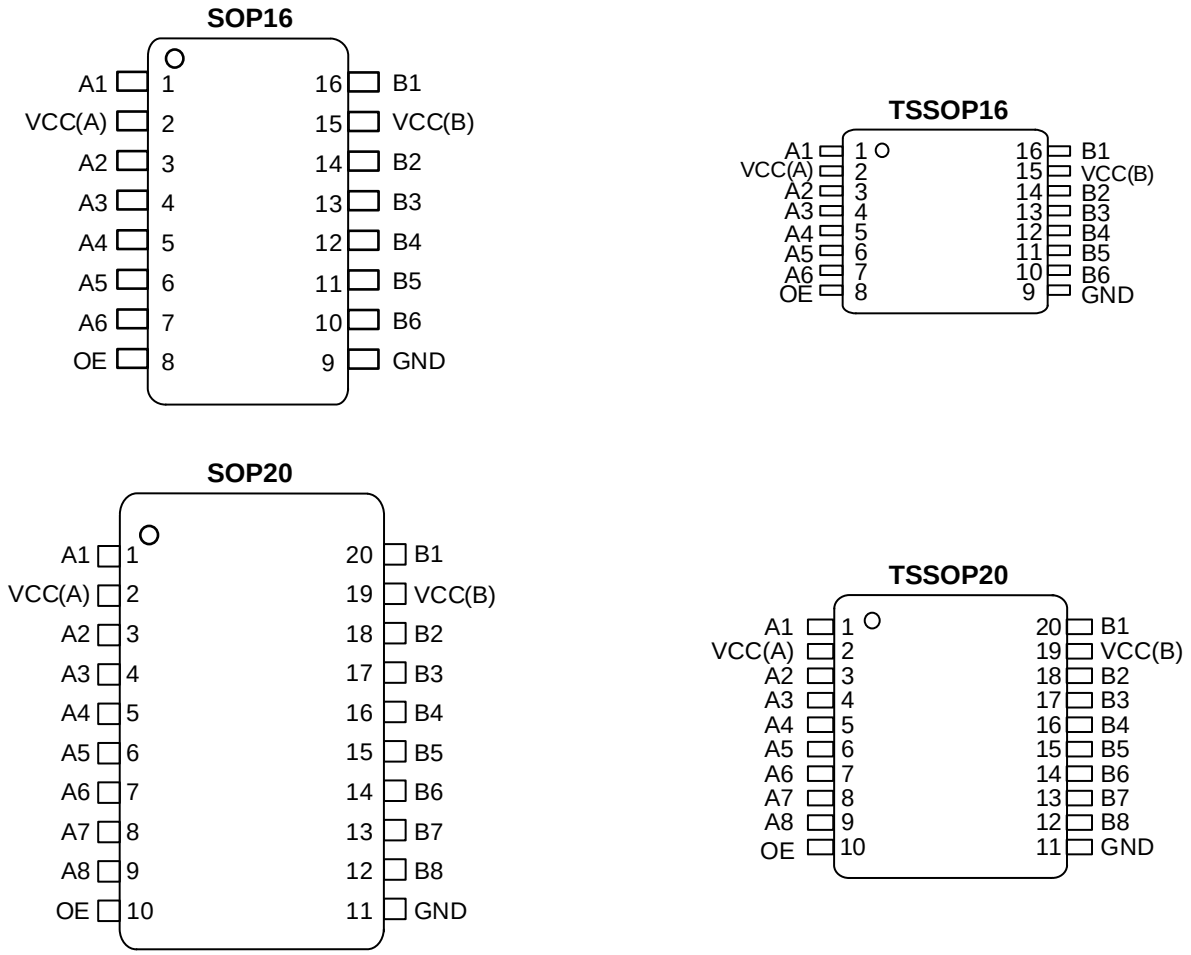


Figure 6-1 Pin configuration

6.2 Pin Function

6.2.1 SOT-23-6L/SOT-363

PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	VCC(A)	P	Supply voltage A
2	GND	G	Ground (0V)
3	A	I/O	Data input or output (referenced to VCC(A))
4	B	I/O	Data input or output (referenced to VCC(B))
5	OE	I	Output enable input (active HIGH; referenced to VCC(A))
6	VCC(B)	P	Supply voltage B

(1) I-Input, O-Output, P-Power, G-Ground

6.2.2 TSSOP8(3x3)/VSSOP8

PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	B2	I/O	Data input or output (referenced to VCC(B))
2	GND	G	Ground (0V)
3	VCC(A)	P	Supply voltage A
4	A2	I/O	Data input or output (referenced to VCC(A))
5	A1	I/O	Data input or output (referenced to VCC(A))
6	OE	I	Output enable input (active HIGH; referenced to VCC(A))
7	VCC(B)	P	Supply voltage B
8	B1	I/O	Data input or output (referenced to VCC(B))

(1) I-Input, O-Output, P-Power, G-Ground

6.2.3 SOP14/TSSOP14/QFN3x2.5-14L/QFN3.5x3.5-14L

PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	VCC(A)	P	Supply voltage A
2	A1	I/O	Data input or output (referenced to VCC(A))
3	A2	I/O	Data input or output (referenced to VCC(A))
4	A3	I/O	Data input or output (referenced to VCC(A))
5	A4	I/O	Data input or output (referenced to VCC(A))
6	N.C.	-	Not connected
7	GND	G	Ground (0V)
8	OE	I	Output enable input (active HIGH; referenced to VCC(A))
9	N.C.	-	Not connected
10	B4	I/O	Data input or output (referenced to VCC(B))
11	B3	I/O	Data input or output (referenced to VCC(B))
12	B2	I/O	Data input or output (referenced to VCC(B))
13	B1	I/O	Data input or output (referenced to VCC(B))
14	VCC(B)	P	Supply voltage B

(1) I-Input, O-Output, P-Power, G-Ground

6.2.4 SOP16/TSSOP16

PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	A1	I/O	Data input or output (referenced to VCC(A))
2	VCC(A)	P	Supply voltage A
3	A2	I/O	Data input or output (referenced to VCC(A))
4	A3	I/O	Data input or output (referenced to VCC(A))
5	A4	I/O	Data input or output (referenced to VCC(A))
6	A5	I/O	Data input or output (referenced to VCC(A))
7	A6	I/O	Data input or output (referenced to VCC(A))
8	OE	I	Output enable input (active HIGH; referenced to VCC(A))
9	GND	G	Ground (0V)
10	B6	I/O	Data input or output (referenced to VCC(B))
11	B5	I/O	Data input or output (referenced to VCC(B))
12	B4	I/O	Data input or output (referenced to VCC(B))
13	B3	I/O	Data input or output (referenced to VCC(B))
14	B2	I/O	Data input or output (referenced to VCC(B))
15	VCC(B)	P	Supply voltage B
16	B1	I/O	Data input or output (referenced to VCC(B))

(1) I-Input, O-Output, P-Power, G-Ground

6.2.5 SOP20/TSSOP20

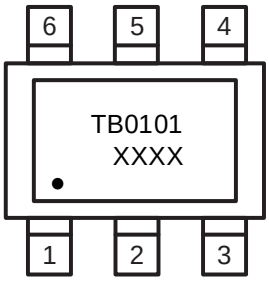
PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	A1	I/O	Data input or output (referenced to VCC(A))
2	VCC(A)	P	Supply voltage A
3	A2	I/O	Data input or output (referenced to VCC(A))
4	A3	I/O	Data input or output (referenced to VCC(A))
5	A4	I/O	Data input or output (referenced to VCC(A))
6	A5	I/O	Data input or output (referenced to VCC(A))
7	A6	I/O	Data input or output (referenced to VCC(A))
8	A7	I/O	Data input or output (referenced to VCC(A))
9	A8	I/O	Data input or output (referenced to VCC(A))
10	OE	I	Output enable input (active HIGH; referenced to VCC(A))
11	GND	G	Ground (0V)
12	B8	I/O	Data input or output (referenced to VCC(B))
13	B7	I/O	Data input or output (referenced to VCC(B))
14	B6	I/O	Data input or output (referenced to VCC(B))
15	B5	I/O	Data input or output (referenced to VCC(B))
16	B4	I/O	Data input or output (referenced to VCC(B))
17	B3	I/O	Data input or output (referenced to VCC(B))
18	B2	I/O	Data input or output (referenced to VCC(B))
19	VCC(B)	P	Supply voltage B
20	B1	I/O	Data input or output (referenced to VCC(B))

(1) I-Input, O-Output, P-Power, G-Ground

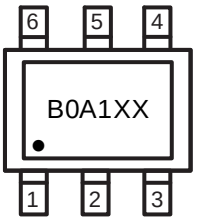
6.3 Marking Information

6.3.1 CJTB0101

SOT-23-6L



SOT-363



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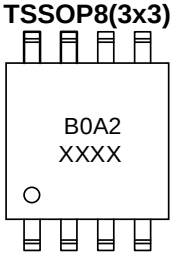
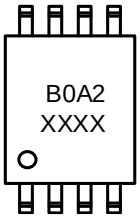
6.3.2 CJTB0102

TSSOP8(3x3)



VSSOP8



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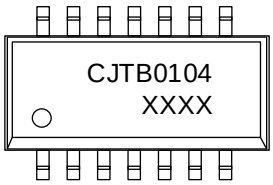
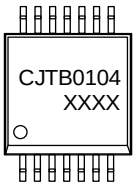
6.3.3 CJTB0104

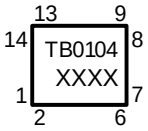
SOP14



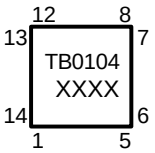
TSSOP14



QFN3x2.5-14L



QFN3.5x3.5-14L



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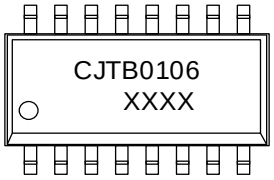
6.3.4 CJTB0106

SOP16



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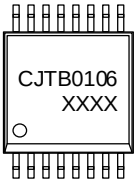

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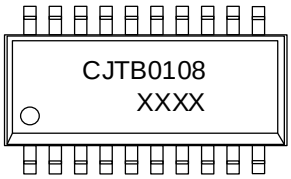
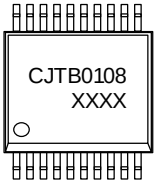
6.3.5 CJTB0108

SOP20



TSSOP20



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7 Specifications

7.1 Absolute Maximum Ratings

T_{amb}=25°C, all voltage referenced to GND, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC(A)}$	Supply voltage A	-	-0.5	+6.5	V
$V_{CC(B)}$	Supply voltage B	-	-0.5	+6.5	V
V_I	Input voltage	- (1)	-0.5	+6.5	V
V_O	Output voltage	Power-down or 3-state mode(1)	-0.5	+6.5	V
		Active mode (1) (2) (3)	-0.5	V_{CCO}+0.5	V
I_{IK}	Input clamping current	V_I<0V	-50	-	mA
I_{OK}	Output clamping current	V_O<0V	-50	-	mA
I_O	Output current	V_O=0V to V_{CCO}(2)	-	±50	mA
I_{CC}	Supply current	$I_{CC(A)}$ or $I_{CC(B)}$	-	100	mA
I_{GND}	Ground current	-	-100	-	mA
T_{stg}	Storage temperature	-	-65	+150	°C
P_{tot}	Total power dissipation	-	-	500	mW
T_L	Soldering temperature	10s	-	260	°C

(1) The minimum input and minimum output voltage ratings may be exceeded if the input and output current ratings are observed.

(2) V_{CCO} is the supply voltage associated with the output.

(3) V_{CCO}+0.5V should not exceed 6.5V.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{CC(A)}$	Supply voltage A	-		1.2	-	3.6	V
$V_{CC(B)}$	Supply voltage B	-		1.65	-	5.5	V
V_I	Input voltage	-		0	-	5.5	V
V_O	Output voltage	Power-down or 3-state mode; $V_{CC(A)}$=1.2V to 3.6V; $V_{CC(B)}$=1.65V to 5.5V	A port	0	-	3.6	V
			B port	0	-	5.5	V
T_{amb}	Ambient temperature	-		-40	-	+125	°C
Δt/ΔV	Input transition rise and fall rate	$V_{CC(A)}$=1.2V to 3.6V;$V_{CC(B)}$=1.65V to 5.5V		-	-	40	ns/V

Note:

(1) The A and B sides of an unused I/O pair must be held in the same state, both at V_{CCI} or both at GND.

(2) $V_{CC(A)}$ must be less than or equal to $V_{CC(B)}$.

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM) (1)	±8000	V

(1) JEDEC document JEP155 states that 500-V H1BM allows safe manufacturing with a standard ESD control process.

7.4 Electrical Characteristics

7.4.1 DC Characteristics 1

T_{amb}=25°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{OH}	HIGH-level output voltage	A port; $V_{CC(A)}$=1.2V; I_O=-20uA		-	1.1	-	V
V_{OL}	LOW-level output voltage	A port; $V_{CC(A)}$=1.2V; I_O=20uA		-	0.09	-	V
I_I	Input leakage current	OE input; V_I=0V to 3.6V; $V_{CC(A)}$=1.2V to 3.6V; $V_{CC(B)}$=1.65V to 5.5V		-	-	±1	uA
I_{OZ}	OFF-state output current	A or B port; V_O=0V or V_{CCO}; $V_{CC(A)}$=1.2V to 3.6V; $V_{CC(B)}$=1.65V to 5.5V		-	-	±1	uA
I_{OFF}	Power-off leakage current	A port; V_I or V_O=0V to 3.6V; $V_{CC(A)}$=0V; $V_{CC(B)}$=0V to 5.5V		-	-	±1	uA
		B port; V_I or V_O=0V to 5.5V; $V_{CC(B)}$=0V; $V_{CC(A)}$=0V to 3.6V		-	-	±1	uA
C_I	Input capacitance	OE input; $V_{CC(A)}$=1.2V to 3.6V; $V_{CC(B)}$=1.65V to 5.5V		-	5	-	pF
$C_{I/O}$	Input/output capacitance	A port; $V_{CC(A)}$=1.2V to 3.6V; $V_{CC(B)}$=1.65V to 5.5V		-	5	-	pF
		B port; $V_{CC(A)}$=1.2V to 3.6V; $V_{CC(B)}$=1.65V to 5.5V		-	8	-	pF
$I_{CC(A)}$	Supply current	$V_{CC(A)}$=1.2V	$V_{CC(B)}$=1.8V	-	10	-	nA
			$V_{CC(B)}$=2.5V	-	10	-	nA
			$V_{CC(B)}$=3.3V	-	10	-	nA
			$V_{CC(B)}$=5.0V	-	10	-	nA
		$V_{CC(A)}$=1.5V	$V_{CC(B)}$=1.8V	-	10	-	nA
			$V_{CC(B)}$=2.5V	-	10	-	nA
			$V_{CC(B)}$=3.3V	-	10	-	nA
			$V_{CC(B)}$=5.0V	-	10	-	nA
		$V_{CC(A)}$=1.8V	$V_{CC(B)}$=1.8V	-	10	-	nA
			$V_{CC(B)}$=2.5V	-	10	-	nA
			$V_{CC(B)}$=3.3V	-	10	-	nA
			$V_{CC(B)}$=5.0V	-	10	-	nA
		$V_{CC(A)}$=2.5V	$V_{CC(B)}$=1.8V	-	-	-	nA
			$V_{CC(B)}$=2.5V	-	10	-	nA
			$V_{CC(B)}$=3.3V	-	10	-	nA
			$V_{CC(B)}$=5.0V	-	10	-	nA
		$V_{CC(A)}$=3.3V	$V_{CC(B)}$=1.8V	-	-	-	nA
			$V_{CC(B)}$=2.5V	-	-	-	nA
			$V_{CC(B)}$=3.3V	-	10	-	nA
			$V_{CC(B)}$=5.0V	-	10	-	nA
$I_{CC(B)}$		$V_{CC(A)}$=1.2V	$V_{CC(B)}$=1.8V	-	10	-	nA
			$V_{CC(B)}$=2.5V	-	10	-	nA

			$V_{CC(B)}$=3.3V	-	20	-	nA
			$V_{CC(B)}$=5.0V	-	1050	-	nA
		$V_{CC(A)}$=1.5V	$V_{CC(B)}$=1.8V	-	10	-	nA
			$V_{CC(B)}$=2.5V	-	10	-	nA
			$V_{CC(B)}$=3.3V	-	10	-	nA
			$V_{CC(B)}$=5.0V	-	150	-	nA
		$V_{CC(A)}$=1.8V	$V_{CC(B)}$=1.8V	-	10	-	nA
			$V_{CC(B)}$=2.5V	-	10	-	nA
			$V_{CC(B)}$=3.3V	-	10	-	nA
			$V_{CC(B)}$=5.0V	-	350	-	nA
		$V_{CC(A)}$=2.5V	$V_{CC(B)}$=1.8V	-	-	-	nA
			$V_{CC(B)}$=2.5V	-	10	-	nA
			$V_{CC(B)}$=3.3V	-	10	-	nA
			$V_{CC(B)}$=5.0V	-	40	-	nA
		$V_{CC(A)}$=3.3V	$V_{CC(B)}$=1.8V	-	-	-	nA
			$V_{CC(B)}$=2.5V	-	-	-	nA
			$V_{CC(B)}$=3.3V	-	10	-	nA
			$V_{CC(B)}$=5.0V	-	10	-	nA

7.4.2 DC Characteristics 2

T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{IH}	HIGH-level input voltage	A or B port and OE input	$V_{CC(A)}$=1.2V to 3.6V; $V_{CC(B)}$=1.65V to 5.5V	0.65V_{CCI}	-	-	V
V_{IL}	LOW-level input voltage	A or B port and OE input	$V_{CC(A)}$=1.2V to 3.6V; $V_{CC(B)}$=1.65V to 5.5V	-	-	0.35V_{CCI}	V
V_{OH}	HIGH-level output voltage	A or B port; I_O=-20uA;	A port; $V_{CC(A)}$=1.4V to 3.6V;	V_{CCO}-0.4	-	-	V
			B port; $V_{CC(B)}$=1.65V to 5.5V	V_{CCO}-0.4	-	-	V
V_{OL}	LOW-level output voltage	A or B port; I_O=20uA;	A port; $V_{CC(A)}$=1.4V to 3.6V;	-	-	0.4	V
			B port; $V_{CC(B)}$=1.65V to 5.5V	-	-	0.4	V
I_I	Input leakage current	OE input; V_I=0V to 3.6V; $V_{CC(A)}$=1.2V to 3.6V; $V_{CC(B)}$=1.65V to 5.5V		-	-	±2	uA
I_{OZ}	OFF-state output current	A or B port; V_O=0V or V_{CCO}; $V_{CC(A)}$=1.2V to 3.6V; $V_{CC(B)}$=1.65V to 5.5V		-	-	±2	uA
I_{OFF}	Power-off leakage current	A port; V_I or V_O=0V to 3.6V; $V_{CC(A)}$=0V; $V_{CC(B)}$=0V to 5.5V		-	-	±2	uA
		B port; V_I or V_O=0V to 5.5V; $V_{CC(B)}$=0V; $V_{CC(A)}$=0V to 3.6V		-	-	±2	uA
I_{CC}	Supply current	V_I=0V or V_{CCI}; I_O=0A					
		$I_{CC(A)}$	OE=LOW; $V_{CC(A)}$=1.4V to 3.6V; $V_{CC(B)}$=1.65V to 5.5V	-	-	15	uA
			OE=HIGH; $V_{CC(A)}$=1.4V to 3.6V; $V_{CC(B)}$=1.65V to 5.5V	-	-	15	uA
			$V_{CC(A)}$=3.6V; $V_{CC(B)}$=0V	-	-	15	uA
			$V_{CC(A)}$=0V; $V_{CC(B)}$=5.5V	-	-	-15	uA
		$I_{CC(B)}$	OE=LOW; $V_{CC(A)}$=1.4V to 3.6V; $V_{CC(B)}$=1.65V to 5.5V	-	-	18	uA
			OE=HIGH; $V_{CC(A)}$=1.4V to 3.6V; $V_{CC(B)}$=1.65V to 5.5V	-	-	18	uA
			$V_{CC(A)}$=3.6V; $V_{CC(B)}$=0V	-	-	-15	uA
			$V_{CC(A)}$=0V; $V_{CC(B)}$=5.5V	-	-	12	uA
		$I_{CC(A)}$+$I_{CC(B)}$	$V_{CC(A)}$=1.4V to 3.6V; $V_{CC(B)}$=1.65V to 5.5V	-	-	30	uA

Note:

(1) V_{CCI} is the supply voltage associated with the input.

(2) V_{CCO} is the supply voltage associated with the output.

7.4.3 DC Characteristics 3

T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{IH}	HIGH-level input voltage	A or B port and OE input	$V_{CC(A)}$=1.2V to 3.6V; $V_{CC(B)}$=1.65V to 5.5V	0.65V_{CCI}	-	-	V
V_{IL}	LOW-level input voltage	A or B port and OE input	$V_{CC(A)}$=1.2V to 3.6V; $V_{CC(B)}$=1.65V to 5.5V	-	-	0.35V_{CCI}	V
V_{OH}	HIGH-level output voltage	A or B port; I_O=-20uA;	A port; $V_{CC(A)}$=1.4V to 3.6V;	V_{CCO}-0.4	-	-	V
			B port; $V_{CC(B)}$=1.65V to 5.5V	V_{CCO}-0.4	-	-	V
V_{OL}	LOW-level output voltage	A or B port; I_O=20uA;	A port; $V_{CC(A)}$=1.4V to 3.6V;	-	-	0.4	V
			B port; $V_{CC(B)}$=1.65V to 5.5V	-	-	0.4	V
I_I	Input leakage current	OE input; V_I=0V to 3.6V; $V_{CC(A)}$=1.2V to 3.6V; $V_{CC(B)}$=1.65V to 5.5V		-	-	±5	uA
I_{OZ}	OFF-state output current	A or B port; V_O=0V or V_{CCO}; $V_{CC(A)}$=1.2V to 3.6V; $V_{CC(B)}$=1.65V to 5.5V		-	-	±10	uA
I_{OFF}	Power-off leakage current	A port; V_I or V_O=0V to 3.6V; $V_{CC(A)}$=0V; $V_{CC(B)}$=0V to 5.5V		-	-	±10	uA
		B port; V_I or V_O=0V to 5.5V; $V_{CC(B)}$=0V; $V_{CC(A)}$=0V to 3.6V		-	-	±10	uA
I_{CC}	Supply current	V_I=0V or V_{CCI}; I_O=0A					
		$I_{CC(A)}$	OE=LOW; $V_{CC(A)}$=1.4V to 3.6V; $V_{CC(B)}$=1.65V to 5.5V	-	-	18	uA
			OE=HIGH; $V_{CC(A)}$=1.4V to 3.6V; $V_{CC(B)}$=1.65V to 5.5V	-	-	20	uA
			$V_{CC(A)}$=3.6V; $V_{CC(B)}$=0V	-	-	18	uA
			$V_{CC(A)}$=0V; $V_{CC(B)}$=5.5V	-	-	-18	uA
		$I_{CC(B)}$	OE=LOW; $V_{CC(A)}$=1.4V to 3.6V; $V_{CC(B)}$=1.65V to 5.5V	-	-	20	uA
			OE=HIGH; $V_{CC(A)}$=1.4V to 3.6V; $V_{CC(B)}$=1.65V to 5.5V	-	-	65	uA
			$V_{CC(A)}$=3.6V; $V_{CC(B)}$=0V	-	-	-18	uA
			$V_{CC(A)}$=0V; $V_{CC(B)}$=5.5V	-	-	18	uA
		$I_{CC(A)}$+$I_{CC(B)}$	$V_{CC(A)}$=1.4V to 3.6V; $V_{CC(B)}$=1.65V to 5.5V	-	-	85	uA

Note:

(1) V_{CCI} is the supply voltage associated with the input.

(2) V_{CCO} is the supply voltage associated with the output.

7.4.4 AC Characteristics 1

T_{amb}=25°C, $V_{CC(A)}$=1.2V,voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	$V_{CC(B)}$				UNIT
			1.8V	2.5V	3.3V	5.0V	
t_{PHL}	Propagation delay	A to B	19.3	18.1	18.0	18.0	ns
		B to A	22.9	21.5	21.0	21.5	ns
t_{PLH}		A to B	21.8	19.8	19.2	18.7	ns
		B to A	24.5	23.4	22.8	22.8	ns
t_{PZL}, t_{PZH}	Enable time	OE to A; B	500	500	500	500	ns
t_{PLZ}, t_{PHZ}	Disable time	OE to A; No external load(1)	20	20	20	20	ns
		OE to B; No external load(1)	20	18	16	16	ns
		OE to A; See Figure 8-4	101	92	104	91	ns
		OE to B; See Figure 8-4	101	92	104	91	ns
t_{TLH}	Transition time	A port	4.1	4.6	5.2	5.7	ns
		B port	2.0	1.9	1.7	1.7	ns
t_{THL}		A port	11.0	11.9	12.2	12.8	ns
		B port	2.7	2.1	1.9	1.7	ns
$t_{sk(o)}$	Output skew time	Between channels(2)	1.4	0.7	0.6	0.5	ns
t_W	Pulse width	Data inputs	22	22	22	22	ns
f_{data}	Data rate	-	45	45	45	45	Mbps

(1) These values are guaranteed by design.

(2) Skew between any two outputs of the same package switching in the same direction.

7.4.5 AC Characteristics 2

T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	$V_{CC(B)}$								UNIT
			1.8V±0.15V		2.5V±0.2V		3.3V±0.3V		5.0V±0.5V		
			MIN.	MAX	MIN.	MAX	MIN.	MAX	MIN.	MAX	
$V_{CC(A)}$=1.5V±0.1V											
t_{PLH}, t_{PHL}	Propagation delay	A to B	1.4	26.4	1.2	22.8	1.1	21.4	0.8	21.0	ns
		B to A	0.9	25.4	0.7	21.6	0.4	19.6	0.3	18.0	ns
t_{PZL}, t_{PZH}	Enable time	OE to A, B	-	1	-	1	-	1	-	1	us
t_{PLZ}, t_{PHZ}	Disable time	OE to A; No external load(1)	3.7	18	3.7	18	3.7	18	3.7	18	ns
		OE to B; No external load(1)	3.7	23	3.5	22	3.0	21	1.7	20	ns
		OE to A; See Figure 8-4	-	320	-	320	-	320	-	320	ns
		OE to B; See Figure 8-4	-	200	-	200	-	200	-	200	ns
t_{THL}, t_{TLH}	Transition time	A port	0.8	5.6	0.8	5.9	0.8	6.8	0.8	6.5	ns
		B port	1.0	4.4	0.7	3.2	0.7	2.9	0.6	2.6	ns
$t_{sk(o)}$	Output skew time	Between channels(2)	-	2.6	-	1.9	-	1.6	-	1.3	ns
t_W	Pulse width	Data inputs	20	-	20	-	20	-	20	-	ns
f_{data}	Data rate	-	-	50	-	50	-	50	-	50	Mbps
$V_{CC(A)}$=1.8V±0.15V											
t_{PLH}, t_{PHL}	Propagation delay	A to B	1.6	21.2	1.4	17.0	1.3	15.6	1.2	15.0	ns
		B to A	1.5	20.2	1.3	15.4	0.8	13.8	0.5	13.2	ns
t_{PZL}, t_{PZH}	Enable time	OE to A, B	-	1	-	1	-	1	-	1	us
t_{PLZ}, t_{PHZ}	Disable time	OE to A; No external load(1)	2.9	17	2.9	17	2.9	17	2.9	17	ns
		OE to B; No external load(1)	4.0	22	3.0	22	2.5	21	1.5	20	ns
		OE to A; See Figure 8-4	-	260	-	260	-	260	-	260	ns
		OE to B; See Figure 8-4	-	200	-	200	-	200	-	200	ns
t_{THL}, t_{TLH}	Transition time	A port	0.7	4.2	0.7	3.8	1.0	3.5	0.7	3.2	ns
		B port	1.0	4.5	0.7	3.5	0.7	3.0	0.6	2.6	ns
$t_{sk(o)}$	Output skew time	Between channels(2)	-	0.8	-	0.8	-	0.8	-	0.8	ns
t_W	Pulse width	Data inputs	22	-	18	-	17	-	17	-	ns
f_{data}	Data rate	-	-	45	-	55	-	60	-	60	Mbps
$V_{CC(A)}$=2.5V±0.2V											
t_{PLH}, t_{PHL}	Propagation	A to B	-	-	1.1	12.2	1.0	11.0	0.9	10.0	ns

	delay	B to A	-	-	1.0	11.6	0.6	10.2	0.3	9.0	ns
t_{PZL}, t_{PZH}	Enable time	OE to A; B	-	-	-	1	-	1	-	1	us
t_{PLZ}, t_{PHZ}	Disable time	OE to A; No external load(1)	-	-	2.5	12	2.5	12	2.5	11	ns
		OE to B; No external load(1)	-	-	2.0	17	2.8	16	1.2	15	ns
		OE to A; See Figure 8-4	-	-	-	200	-	200	-	200	ns
		OE to B; See Figure 8-4	-	-	-	200	-	200	-	200	ns
t_{THL}, t_{TLH}	Transition time	A port	-	-	0.8	3.0	0.6	3.0	0.5	3.5	ns
		B port	-	-	0.6	3.2	0.7	3.0	0.6	2.7	ns
$t_{sk(o)}$	Output skew time	Between channels(2)	-	-	-	0.4	-	0.3	-	0.3	ns
t_W	Pulse width	Data inputs	-	-	13	-	11	-	10	-	ns
f_{data}	Data rate	-	-	-	-	80	-	90	-	100	Mbps
$V_{CC(A)}$=3.3V±0.3V											
t_{PLH}, t_{PHL}	Propagation delay	A to B	-	-	-	-	0.9	9.2	0.8	8.2	ns
		B to A	-	-	-	-	0.5	8.4	0.2	7.2	ns
t_{PZL}, t_{PZH}	Enable time	OE to A, B	-	-	-	-	-	1	-	1	us
t_{PLZ}, t_{PHZ}	Disable time	OE to A; No external load(1)	-	-	-	-	2.1	13	2.0	12	ns
		OE to B; No external load(1)	-	-	-	-	1.0	12	1.7	11	ns
		OE to A; See Figure 8-4	-	-	-	-	-	200	-	200	ns
		OE to B; See Figure 8-4	-	-	-	-	-	200	-	200	ns
t_{THL}, t_{TLH}	Transition time	A port	-	-	-	-	0.5	2.9	0.5	3.0	ns
		B port	-	-	-	-	0.7	3.0	0.6	2.6	ns
$t_{sk(o)}$	Output skew time	Between channels(2)	-	-	-	-	-	0.4	-	0.3	ns
t_W	Pulse width	Data inputs	-	-	-	-	10.0	-	9.0	-	ns
f_{data}	Data rate	-	-	-	-	-	-	100	-	110	Mbps

(1) These values are guaranteed by design.

(2) Skew between any two outputs of the same package switching in the same direction.

7.4.6 AC Characteristics 3

T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	$V_{CC(B)}$								UNIT
			1.8V±0.15V		2.5V±0.2V		3.3V±0.3V		5.0V±0.5V		
			MIN.	MAX	MIN.	MAX	MIN.	MAX	MIN.	MAX	
$V_{CC(A)}$=1.5V±0.1V											
t_{PLH}, t_{PHL}	Propagation delay	A to B	1.4	29.0	1.2	25.0	1.1	23.5	0.8	23.1	ns
		B to A	0.9	27.9	0.7	23.7	0.4	21.5	0.3	19.8	ns
t_{PZL}, t_{PZH}	Enable time	OE to A, B	-	1.0	-	1.0	-	1.0	-	1.0	us
t_{PLZ}, t_{PHZ}	Disable time	OE to A; No external load(1)	3.7	19.8	3.7	19.8	3.7	19.8	3.7	19.8	ns
		OE to B; No external load(1)	3.7	25.3	3.5	24.2	3.0	23.1	1.7	22	ns
		OE to A; See Figure 8-4	-	350	-	350	-	350	-	350	ns
		OE to B; See Figure 8-4	-	220	-	220	-	220	-	220	ns
t_{THL}, t_{TLH}	Transition time	A port	0.8	6.2	0.8	6.2	0.8	7.5	0.8	7.1	ns
		B port	1.0	4.9	0.7	3.5	0.7	3.2	0.6	2.9	ns
$t_{sk(o)}$	Output skew time	Between channels(2)	-	2.9	-	2.1	-	1.8	-	1.5	ns
t_W	Pulse width	Data inputs	30	-	28	-	25	-	25	-	ns
f_{data}	Data rate	-	-	33	-	35	-	40	-	40	Mbps
$V_{CC(A)}$=1.8V±0.15V											
t_{PLH}, t_{PHL}	Propagation delay	A to B	1.6	23.3	1.4	18.6	1.3	17.1	1.2	16.5	ns
		B to A	1.5	22.2	1.2	16.9	0.8	15.2	0.5	14.5	ns
t_{PZL}, t_{PZH}	Enable time	OE to A, B	-	1.0	-	1.0	-	1.0	-	1.0	us
t_{PLZ}, t_{PHZ}	Disable time	OE to A; No external load(1)	2.9	18.7	2.9	18.7	2.9	18.7	2.9	18.7	ns
		OE to B; No external load(1)	4.0	24.0	3.0	24.0	2.5	23.2	1.5	22.0	ns
		OE to A; See Figure 8-4	-	280	-	280	-	280	-	280	ns
		OE to B; See Figure 8-4	-	220	-	220	-	220	-	220	ns
t_{THL}, t_{TLH}	Transition time	A port	0.8	4.6	0.7	4.2	1.0	3.9	0.7	3.5	ns
		B port	1.0	4.9	0.7	3.9	0.7	3.3	0.6	2.9	ns
$t_{sk(o)}$	Output skew time	Between channels(2)	-	0.8	-	0.7	-	0.6	-	0.6	ns
t_W	Pulse width	Data inputs	25	-	20	-	18	-	18	-	ns
f_{data}	Data rate	-	-	40	-	50	-	55	-	55	Mbps
$V_{CC(A)}$=2.5V±0.2V											
t_{PLH}, t_{PHL}	Propagation	A to B	-	-	1.1	13.6	1.0	12.1	0.9	11.0	ns

	delay	B to A	-	-	1.0	12.7	0.6	11.2	0.3	10.0	ns
t_{PZL}, t_{PZH}	Enable time	OE to A; B	-	-	-	1.0	-	1.0	-	1.0	us
t_{PLZ}, t_{PHZ}	Disable time	OE to A; No external load(1)	-	-	2.5	13.2	2.5	13.2	2.5	13.2	ns
		OE to B; No external load(1)	-	-	2.0	18.7	2.8	17.6	1.2	16.5	ns
		OE to A; See Figure 8-4	-	-	-	220	-	220	-	220	ns
		OE to B; See Figure 8-4	-	-	-	220	-	220	-	220	ns
t_{THL}, t_{TLH}	Transition time	A port	-	-	0.8	3.3	0.6	3.3	0.5	3.8	ns
		B port	-	-	0.6	3.5	0.7	3.3	0.6	3.0	ns
$t_{sk(o)}$	Output skew time	Between channels(2)	-	-	-	0.4	-	0.3	-	0.3	ns
t_W	Pulse width	Data inputs	-	-	14	-	13	-	13	-	ns
f_{data}	Data rate	-	-	-	-	70	-	80	-	80	Mbps
$V_{CC(A)}$=3.3V±0.3V											
t_{PLH}, t_{PHL}	Propagation delay	A to B	-	-	-	-	0.9	9.9	0.8	9.0	ns
		B to A	-	-	-	-	0.5	9.3	0.2	8.0	ns
t_{PZL}, t_{PZH}	Enable time	OE to A, B	-	-	-	-	-	1.0	-	1.0	us
t_{PLZ}, t_{PHZ}	Disable time	OE to A; No external load(1)	-	-	-	-	2.1	14.1	2.0	13.1	ns
		OE to B; No external load(1)	-	-	-	-	1.0	13.1	1.7	12.1	ns
		OE to A; See Figure 8-4	-	-	-	-	-	220	-	220	ns
		OE to B; See Figure 8-4	-	-	-	-	-	220	-	220	ns
t_{THL}, t_{TLH}	Transition time	A port	-	-	-	-	0.5	3.2	0.5	3.3	ns
		B port	-	-	-	-	0.7	3.3	0.6	2.9	ns
$t_{sk(o)}$	Output skew time	Between channels(2)	-	-	-	-	-	0.4	-	0.3	ns
t_W	Pulse width	Data inputs	-	-	-	-	10	-	10	-	ns
f_{data}	Data rate	-	-	-	-	-	-	100	-	100	Mbps

(1) These values are guaranteed by design.

(2) Skew between any two outputs of the same package switching in the same direction.

7.4.7 Typical Power Dissipation Capacitance

T_{amb}=-25°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		$V_{CC(A)}$							UNIT
				1.2V	1.2V	1.5V	1.8V	2.5V	2.5V	3.3V	
				$V_{CC(B)}$							
				1.8V	5.0V	1.8V	1.8V	2.5V	5.0V	3.3V-5.0V	
C_{PD}	Power dissipation capacitance	Outputs enabled; OE=$V_{CC(A)}$	A port: (direction A to B)	7.0	6.5	7.2	7.6	7.6	7.0	8.0	pF
			A port: (direction B to A)	9.6	10.0	9.8	10.1	10.5	10.3	10.8	pF
			B port: (direction A to B)	23.3	28.7	23.1	23.1	23.7	25.9	25.9	pF
			B port: (direction B to A)	17.8	25.5	17.1	16.8	17.4	21.0	20.5	pF
		Outputs disabled OE=GND	A port: (direction A to B)	0.2	0.2	0.2	0.3	0.3	0.3	0.3	pF
			A port: (direction B to A)	0.01	0.01	0.01	0.01	0.01	0.01	0.01	pF
			B port: (direction A to B)	0.01	0.02	0.01	0.01	0.01	0.01	0.01	pF
			B port: (direction B to A)	0.2	0.3	0.2	0.2	0.3	0.3	0.3	pF

Note:

(1) C_{PD} is used to determine the dynamic power dissipation (P_D in uW).
$P_D=C_{PD}xV_{CC}^2xf_ixN+\sum(C_LxV_{CC}^2xf_o)$ where:
f_i=input frequency in MHz; f_o=output frequency in MHz;
C_L=load capacitance in pF; V_{CC}=supply voltage in V;
N=number of inputs switching; $\sum(C_LxV_{CC}^2xf_o)$=sum of the outputs.

(2) f_i=10MHz; V_I=GND to V_{CC}; $t_r=t_f$=1ns; C_L=0pF; $R_L=\infty\Omega$.

8 Detailed Description

8.1 Overview

The CJTB010X is an 8-bit, dual supply translating transceiver with auto direction sensing, that enables bidirectional voltage level translation. It features two 8-bit input-output ports (An and Bn), one output enable input (OE) and two supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). $V_{CC(A)}$ can be supplied at any voltage between 1.2V and 3.6V and $V_{CC(B)}$ can be supplied at any voltage between 1.65V and 5.5V, making the device suitable for translating between any of the low voltage nodes (1.2V, 1.5V, 1.8V, 2.5V, 3.3V and 5.0 V).

Pins An and OE are referenced to $V_{CC(A)}$ and pins Bn are referenced to $V_{CC(B)}$. A LOW level at pin OE causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

8.2 Functional Block Diagram

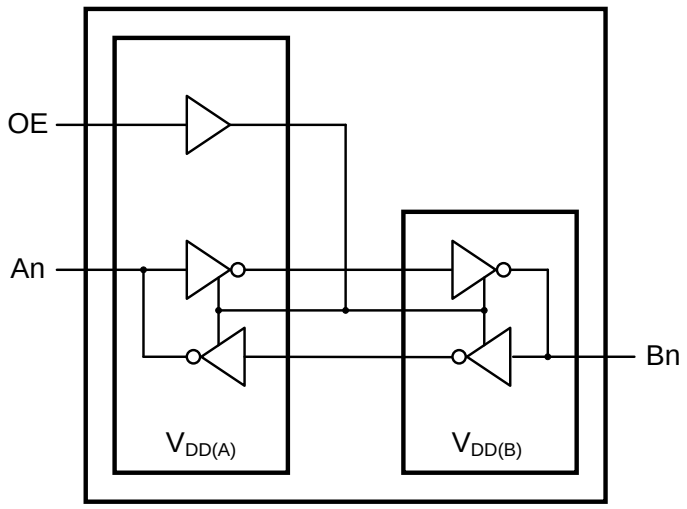


Figure 8-1 Logic symbol (one channel)

8.3 Function Table

SUPPLY VOLTAGE		INPUT	INPUT/OUTPUT	
$V_{CC(A)}$	$V_{CC(B)}$	OE	A	B
1.2V to $V_{CC(B)}$	1.65V to 5.5V	L	Z	Z
1.2V to $V_{CC(B)}$	1.65V to 5.5V	H	Input or output	Output or input
GND	GND	X	Z	Z

Note:
(1) H=HIGH voltage level; L=LOW voltage level; X=don't care; Z=high-impedance OFF-state.
(2) When either $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into power-down mode.

8.4 Testing Circuit

8.4.1 AC Testing Circuit

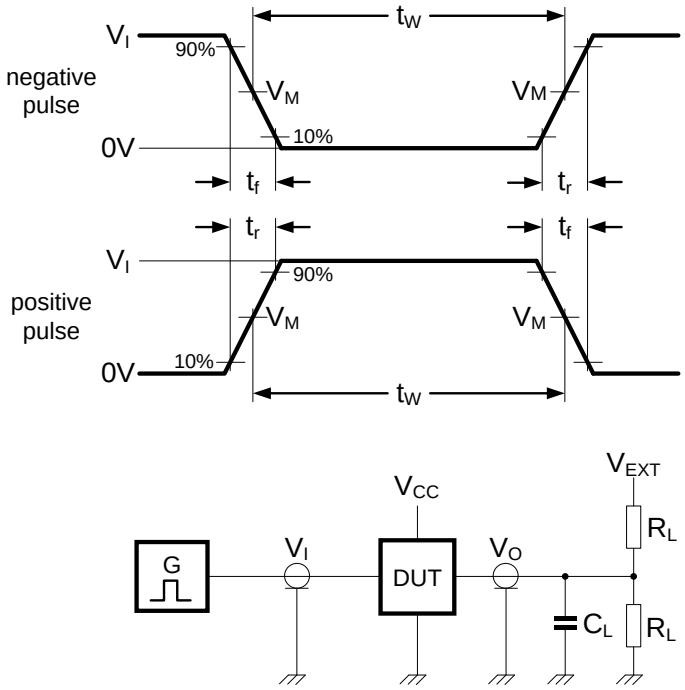


Figure 8-2 Test circuit for measuring switching times

All input pulses are supplied by generators having the following characteristics:

PRR≤10MHz; Z_O=50Ω; dV/dt≥1.0V/ns.

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

V_{EXT}=External voltage for measuring switching times.

8.4.2 AC Testing Waveforms

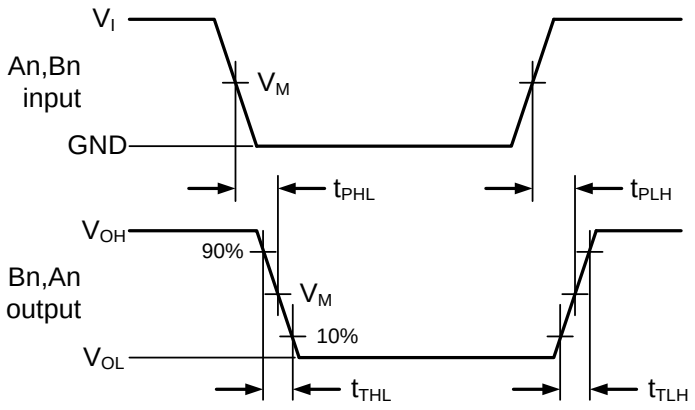


Figure 8-3 The data input (An, Bn) to data output (Bn, An) propagation delay times

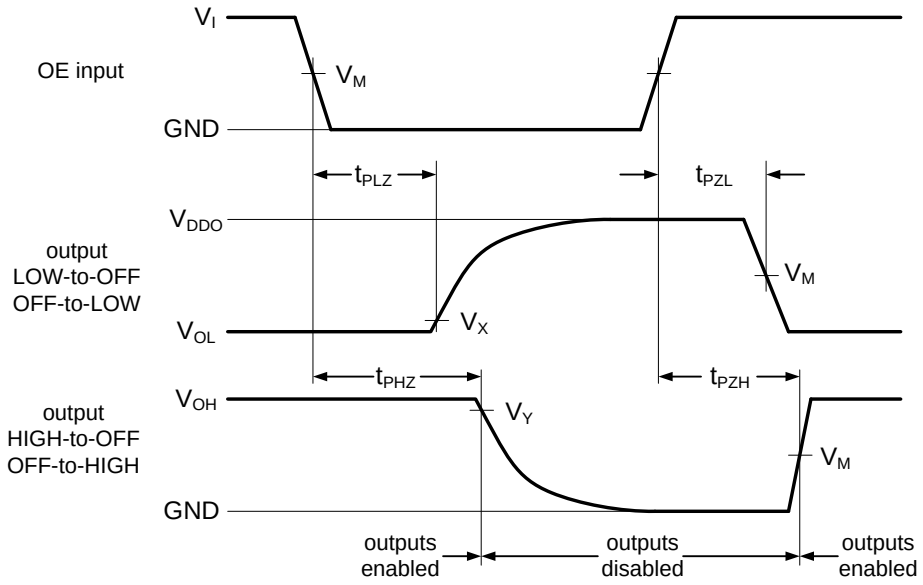


Figure 8-4 3-state enable and disable times

8.4.3 Measurement Points

SUPPLY VOLTAGE	INPUT	OUTPUT		
V_{CCO}	V_M	V_M	V_X	V_Y
1.2V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL}+0.1V	V_{OH}-0.1V
1.5V±0.1V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL}+0.1V	V_{OH}-0.1V
1.8V±0.15V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL}+0.15V	V_{OH}-0.15V
2.5V±0.2V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL}+0.15V	V_{OH}-0.15V
3.3V±0.3V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL}+0.3V	V_{OH}-0.3V
5.0V±0.5V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL}+0.3V	V_{OH}-0.3V

Note:

(1) V_{CCI} is the supply voltage associated with the input.

(2) V_{CCO} is the supply voltage associated with the output.

8.4.4 Test Data

SUPPLY VOLTAGE		INPUT		LOAD		V_{EXT}		
$V_{CC(A)}$	$V_{CC(B)}$	V_I	$\Delta t/\Delta V$	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.2V to 3.6V	1.65V to 5.5V	V_{CCI}	≤1.0ns/V	15pF	50kΩ, 1MΩ	Open	Open	$2V_{CCO}$

Note:

(1) V_{CCI} is the supply voltage associated with the input.

(2) For measuring data rate, pulse width, propagation delay and output rise and fall measurements, R_L=1MΩ.
For measuring enable and disable times, R_L=50kΩ.

(3) V_{CCO} is the supply voltage associated with the output.

9 Typical Application Circuit and Application Note

9.1 Voltage Level-translation Applications

Voltage level-translation applications. The CJTB010X can be used to interface between devices or systems operating at different supply voltages. See Figure 9-1 for a typical operating circuit using the CJTB010X.

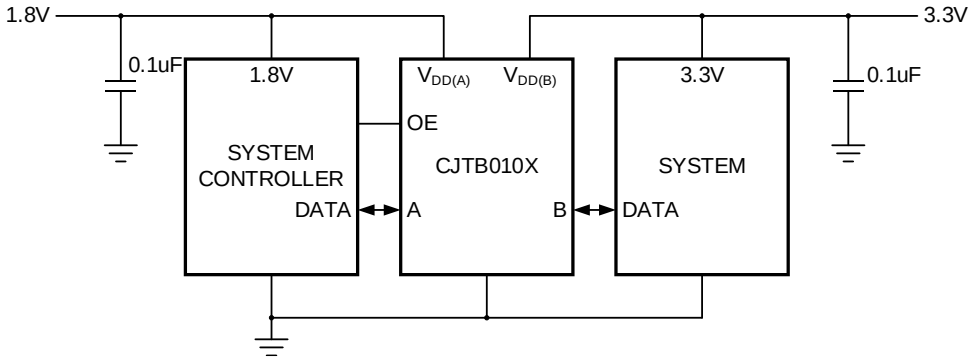


Figure 9-1 Typical operating circuit

9.2 Architecture

The architecture of the CJTB010X is shown in Figure 9-2. The device does not require an extra input signal to control the direction of data flow from A to B or from B to A. In a static state, the output drivers of the CJTB010X can maintain a defined output level, but the output architecture is designed to be weak, so that they can be overdriven by an external driver when data on the bus starts flowing in the opposite direction. The output one shots detect rising or falling edges on the A or B ports. During a rising edge, the one shots turn on the PMOS transistors (T1, T3) for a short duration, accelerating the low-to-high transition. Similarly, during a falling edge, the one shots turn on the NMOS transistors (T2, T4) for a short duration, accelerating the high-to-low transition. During output transitions the typical output impedance is 70Ω at V_{CCO}=1.2V to 1.8V, 50 Ω at V_{CCO}=1.8V to 3.3V and 40Ω at V_{CCO}=3.3V to 5.0V.

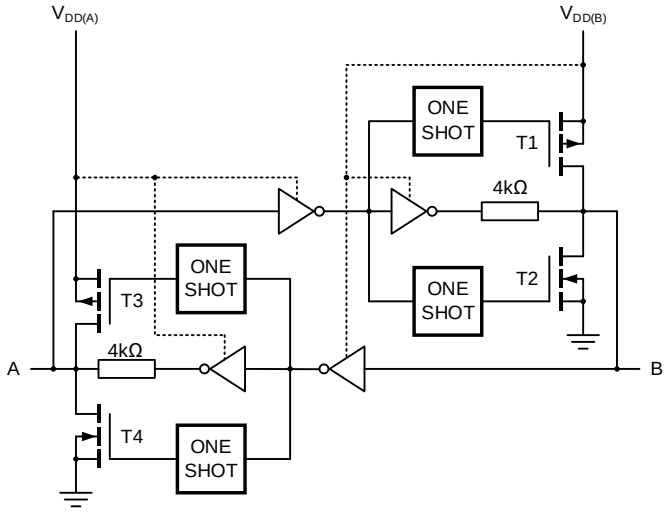
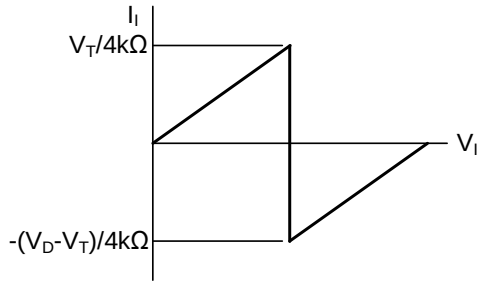


Figure 9-2 Architecture of CJTB010X I/O cell (one channel)

9.3 Input Driver Requirements

For correct operation, the device driving the data I/Os of the CJTB010X must have a minimum drive capability of ±2mA See Figure 9-3 for a plot of typical input current versus input voltage.



V_T: input threshold voltage of the CJTB010X (typically $V_{CCI}/2$).
V_D: supply voltage of the external driver.

Figure 9-3 Typical input current versus input voltage graph

9.4 Power Up

During operation $V_{CC(A)}$ must never be higher than $V_{CC(B)}$, however during power-up $V_{CC(A)} \geq V_{CC(B)}$ does not damage the device, so either power supply can be ramped up first. There is no special power-up sequencing required. The CJTB010X includes circuitry that disables all output ports when either $V_{CC(A)}$ or $V_{CC(B)}$ is switched off.

9.5 Enable and Disable

An output enable input (OE) is used to disable the device. Setting OE=LOW causes all I/Os to assume the high-impedance OFF-state. The disable time (t_{dis} with no external load) indicates the delay between when OE goes LOW and when outputs actually become disabled. The enable time (t_{en}) indicates the amount of time the user must allow for one one-shot circuitry to become operational after OE is taken HIGH. To ensure the high-impedance OFF-state during power-up or power-down, pin OE should be tied to GND through a pull-down resistor, the minimum value of the resistor is determined by the current-sourcing capability of the driver.

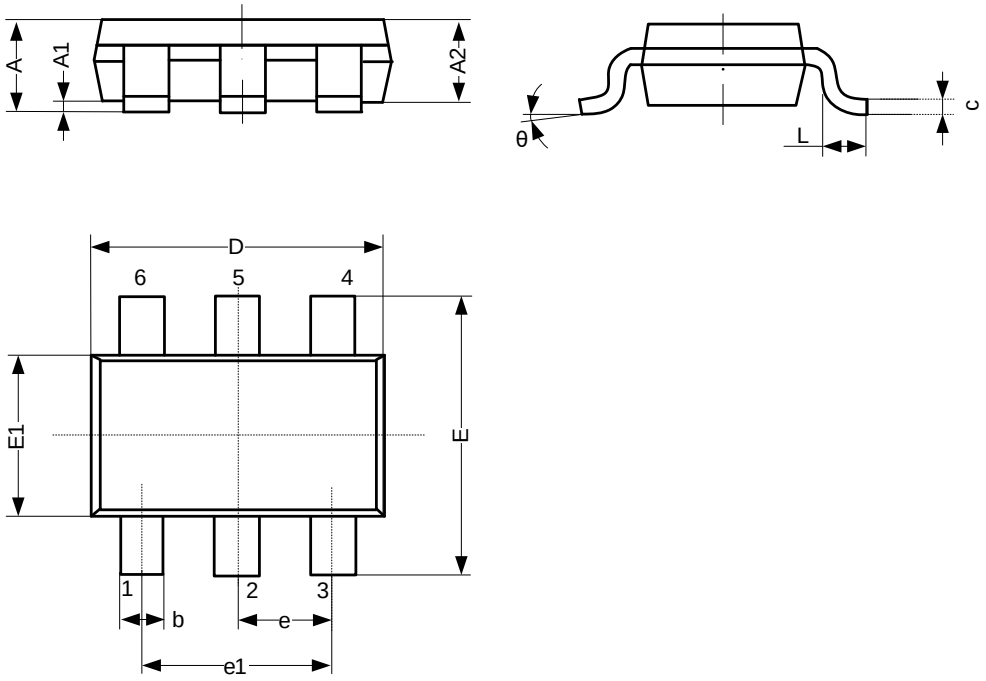
9.6 Pull-up or Pull-down Resistors on I/O Lines

As mentioned previously the CJTB010X is designed with low static drive strength to drive capacitive loads of up to 70pF. To avoid output contention issues, any pull-up or pull-down resistors used must be kept higher than 50kΩ. For this reason the CJTB010X is not recommended for use in open drain driver applications such as 1-Wire or I^2C. For these applications, the CJTS010X level translator is recommended.

10 Mechanical Information

10.1 SOT-23-6L Mechanical Information

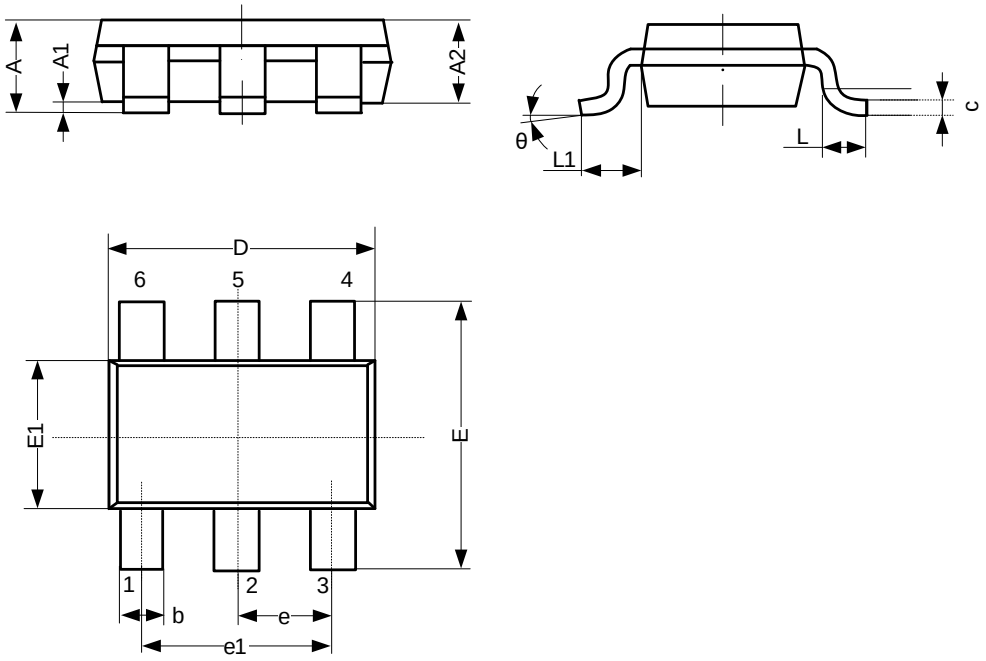
10.1.1 SOT-23-6L Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.25
A1	0.00	-	0.12
A2	1.00	-	1.20
b	0.30	-	0.50
c	0.10	-	0.20
D	2.82	-	3.02
E	2.60	-	3.00
E1	1.50	-	1.70
e	0.95 BSC		
e1	1.80	-	2.00
L	0.30	-	0.60
Θ	0°	-	8°
Unit: mm			

10.2 SOT-363 Mechanical Information

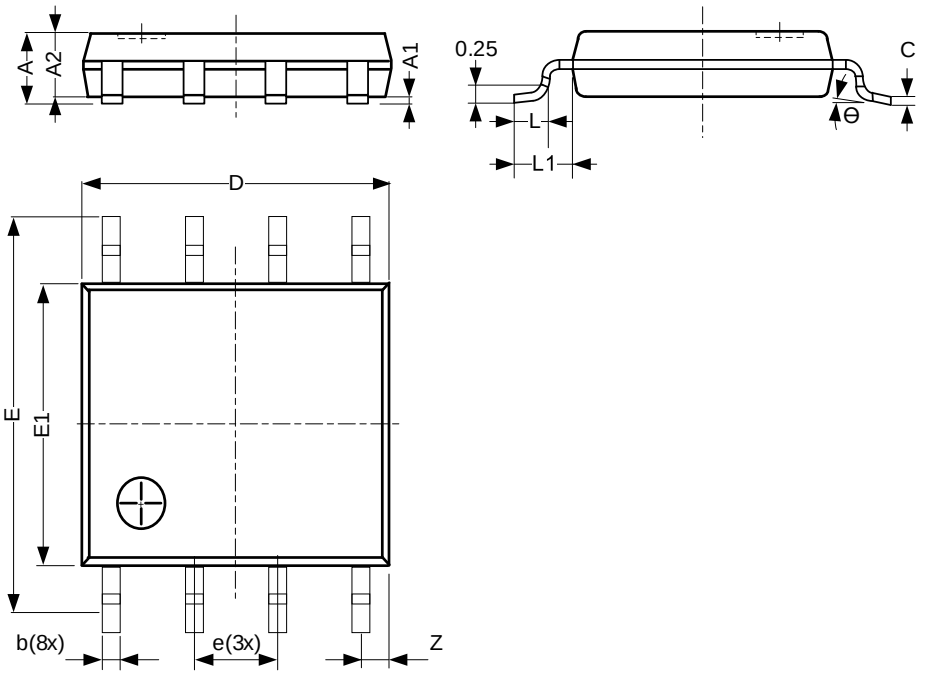
10.2.1 SOT-363 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	0.90	-	1.10
A1	0.00	-	0.10
A2	0.90	-	1.00
b	0.15	-	0.35
c	0.11	-	0.175
D	2.00	-	2.20
E	2.15	-	2.45
E1	1.15	-	1.35
e	0.65 BSC		
e1	1.20	-	1.40
L	0.26	-	0.46
L1	-	0.525	-
Θ	0°	-	8°
Unit: mm			

10.3 TSSOP8(3x3) Mechanical Information

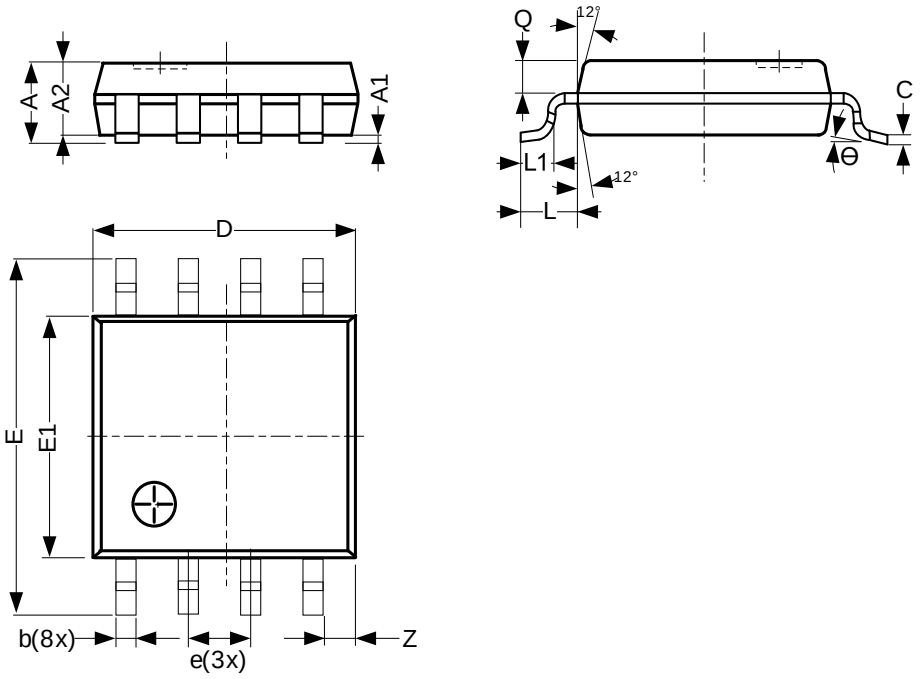
10.3.1 TSSOP8(3x3) Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.10
A1	0	-	0.15
A2	0.75	-	0.95
b	0.22	-	0.38
c	0.08	-	0.18
D	2.90	-	3.10
E	3.90	-	4.10
E1	2.90	-	3.10
e	0.65 BSC		
L	0.33	-	0.47
L1	-	0.50	-
Z	0.35	-	0.70
Θ	0°	-	8°
Unit: mm			

10.4 VSSOP8 Mechanical Information

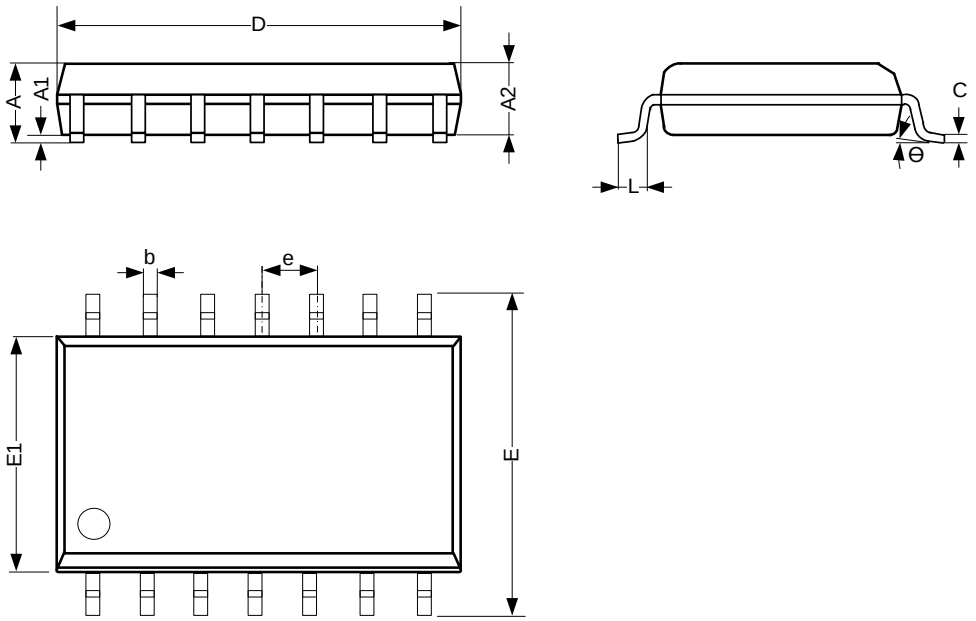
10.4.1 VSSOP8 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.00
A1	0	-	0.15
A2	0.60	-	0.85
Q	0.19	-	0.21
b	0.17	-	0.27
c	0.08	-	0.23
D	1.90	-	2.10
E	3.00	-	3.20
E1	2.20	-	2.40
e	0.50 BSC		
L	-	0.40	-
L1	0.15	-	0.40
Z	0.10	-	0.40
Θ	0°	-	8°
Unit: mm			

10.5 SOP14 Mechanical Information

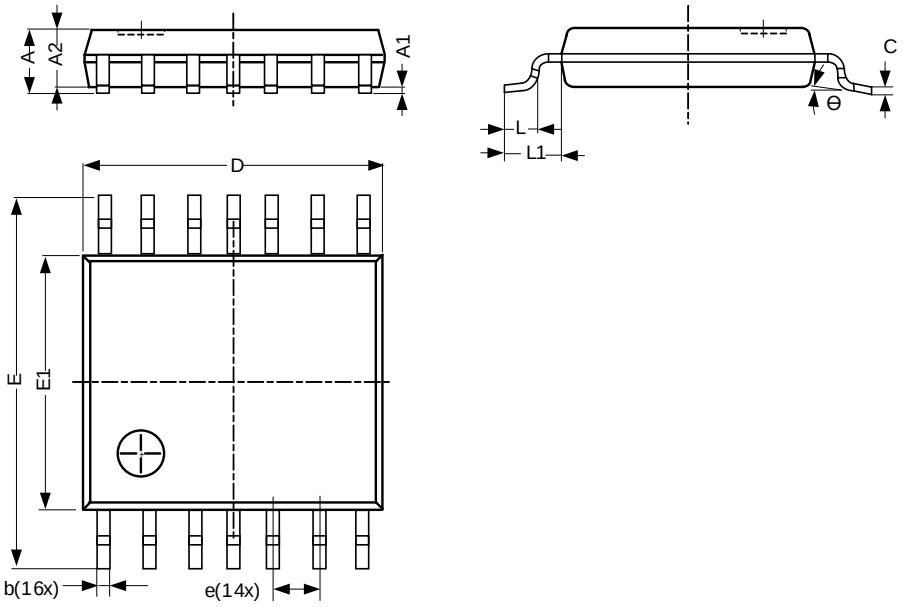
10.5.1 SOP14 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.50	-	1.75
A1	0.05	-	0.25
A2	1.30	-	-
b	0.33	-	0.50
c	0.19	-	0.25
D	8.43	-	8.76
E	5.80	-	6.25
E1	3.75	-	4.00
e	1.27 BSC		
L	0.40	-	0.89
Θ	0°	-	8°
Unit: mm			

10.6 TSSOP14 Mechanical Information

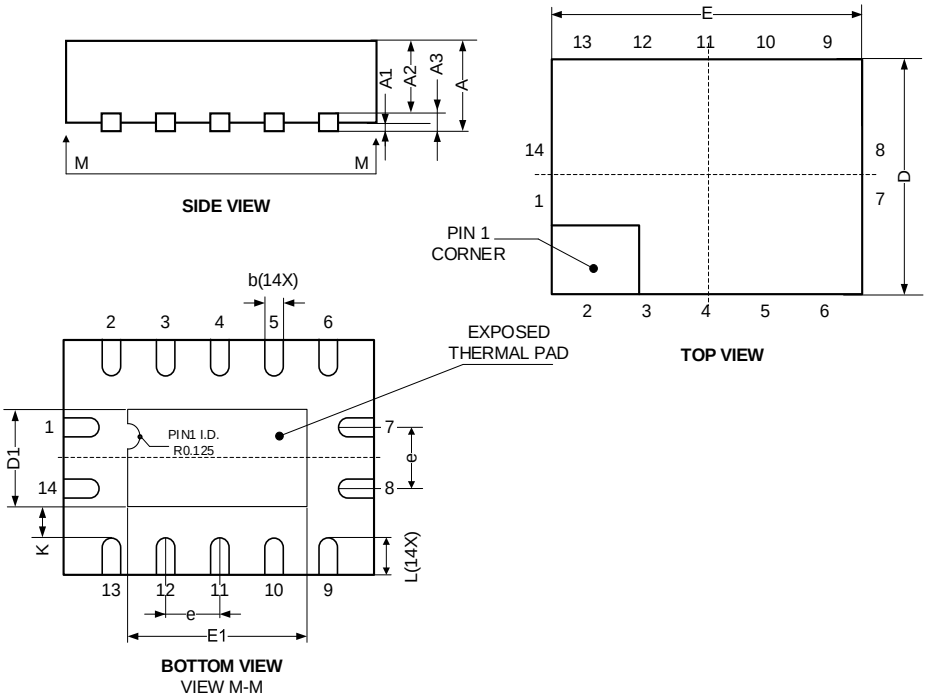
10.6.1 TSSOP14 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	-	5.10
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
L1	-	1.00	-
θ	0°	-	8°
Unit: mm			

10.7 QFN3x2.5-14L Mechanical Information

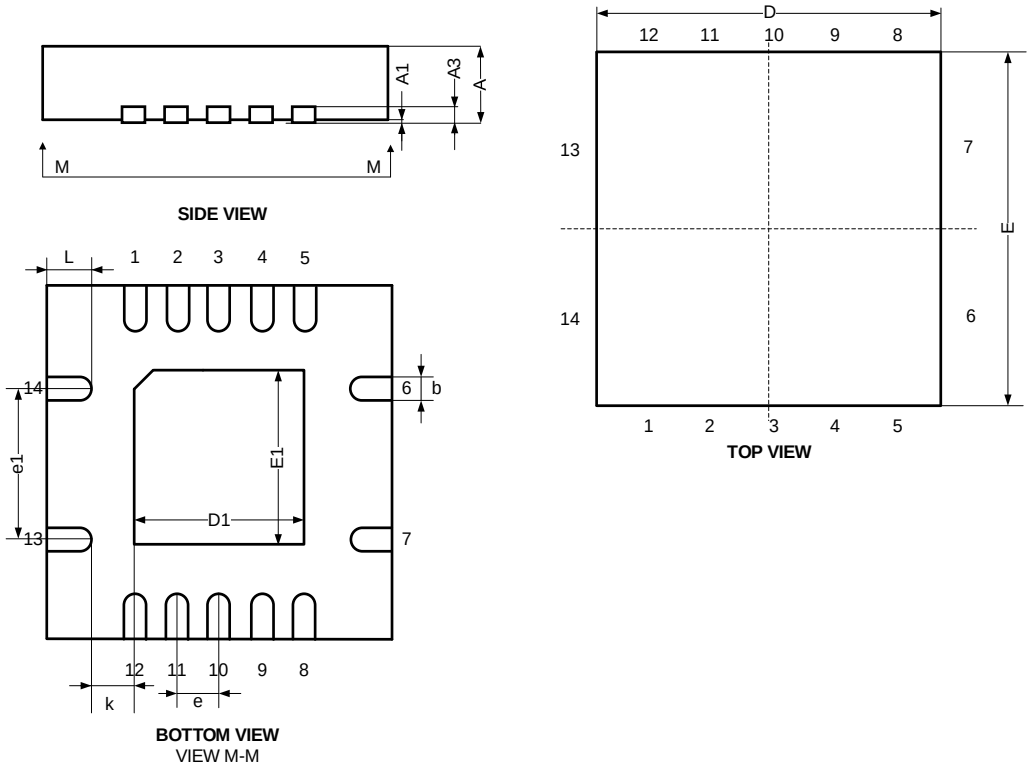
10.7.1 QFN3x2.5-14L Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	0.80	-	1.00
A1	0.00	-	0.05
A2	0.60	-	0.70
A3	-	0.203	-
D	2.40	-	2.60
E	2.90	-	3.10
e	0.50 BSC		
b	0.18	-	0.30
L	0.30	-	0.50
D1	0.85	-	1.15
E1	1.35	-	1.65
K	-	0.35	-
Unit: mm			

10.8 QFN3.5x3.5-14L Mechanical Information

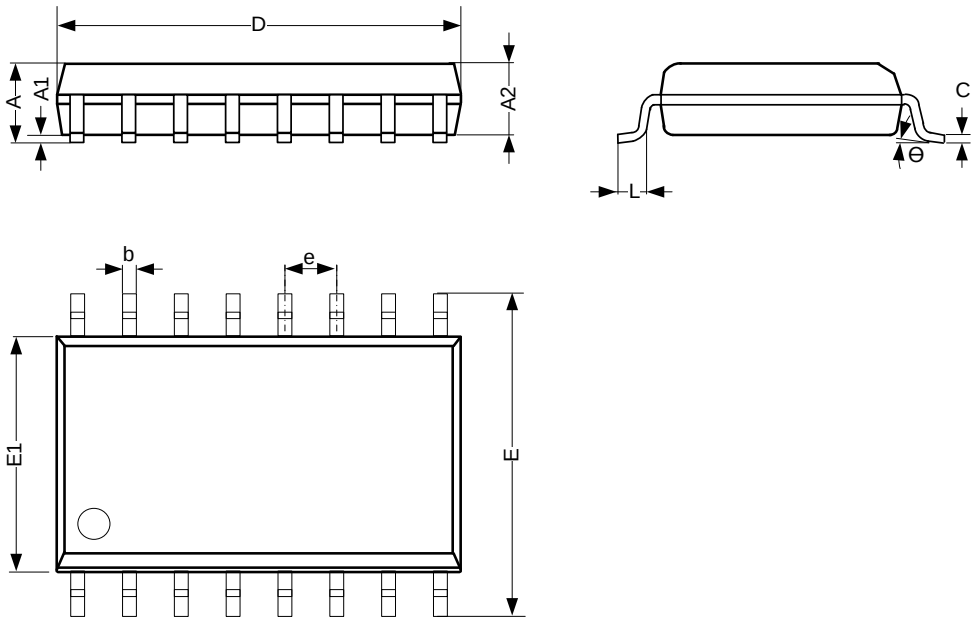
10.8.1 QFN3.5x3.5-14L Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	0.70	-	0.90
A1	0	-	0.05
A3	0.203 REF		
D	3.424	-	3.576
E	3.424	-	3.576
D1	1.95	-	2.15
E1	1.95	-	2.15
k	0.20	-	-
b	0.20	-	0.30
e	0.50 BSC		
e1	1.50 BSC		
L	0.324	-	0.476
Unit: mm			

10.9 SOP16 Mechanical Information

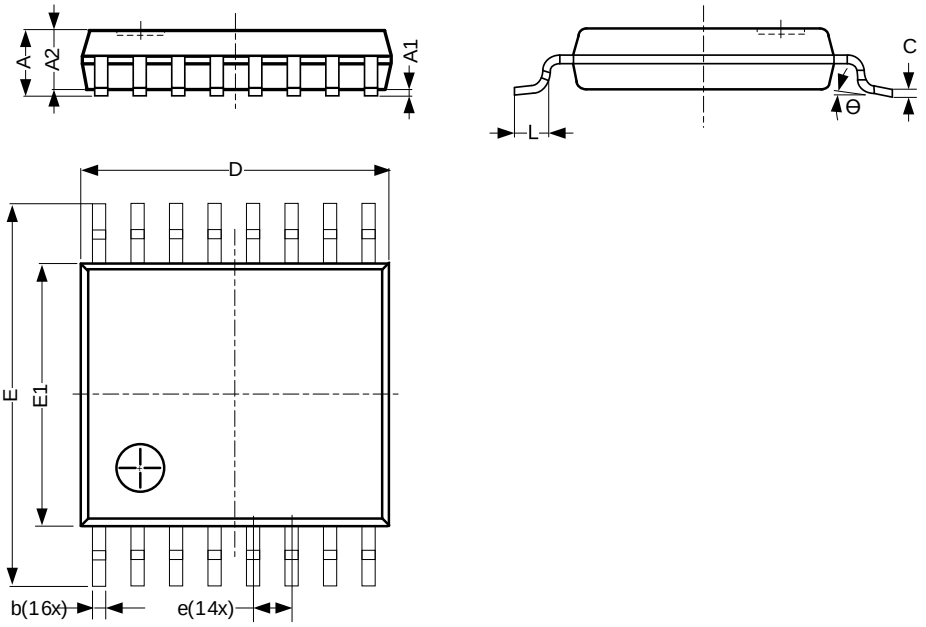
10.9.1 SOP16 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.35	-	1.80
A1	0.10	-	0.25
A2	1.25	-	1.55
b	0.33	-	0.51
c	0.19	-	0.25
D	9.50	-	10.10
E	5.80	-	6.30
E1	3.70	-	4.10
e	1.27 BSC		
L	0.35	-	0.89
Θ	0°	-	8°
Unit: mm			

10.10 TSSOP16 Mechanical Information

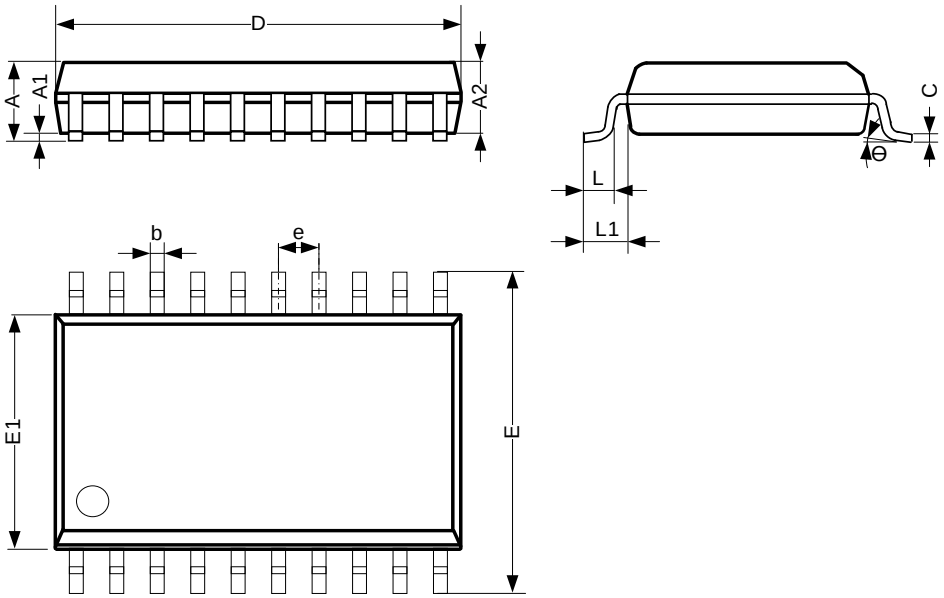
10.10.1 TSSOP16 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	-	5.10
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
Θ	0°	-	8°
Unit: mm			

10.11 SOP20 Mechanical Information

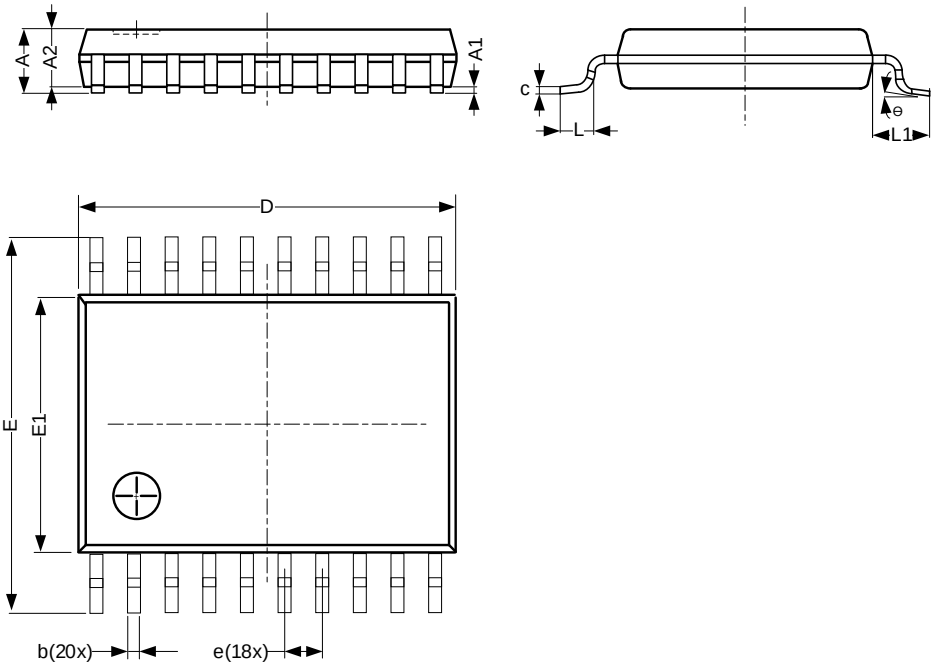
10.11.1 SOP20 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	2.47	-	2.65
A1	0.05	-	0.30
A2	2.20	-	2.44
b	0.35	-	0.50
c	0.15	-	0.30
D	12.54	-	12.94
E	10.00	-	10.60
E1	7.30	-	7.70
e	1.27 BSC		
L	0.40	-	1.05
L1	1.30	-	1.50
Θ	0°	-	8°
Unit: mm			

10.12 TSSOP20 Mechanical Information

10.12.1 TSSOP20 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	6.40	-	6.60
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
L1	-	1.00	-
θ	0°	-	8°
Unit: mm			

11 Notes and Revision History

11.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

11.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

11.3 Revision History

January, 2026: rev -1.1, Change TSSOP8 marking information.

April, 2026: rev -1.2, Update package from TSSOP8 to TSSOP8(3x3).

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

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