

CJWT030JN65AD

Parameter	Value	Unit
$V_{DS@T_J, MAX}$	650	V
$R_{DS(on)TYP}$	26	mΩ
$Q_{g, typ}$	226	nC
I_D	80	A



DESCRIPTION

This device used high Voltage of advanced balanced junction technology, has extremely low $R_{DS(ON)}$ and Gate charge, it fits in applications which require superior power density and outstanding efficiency.

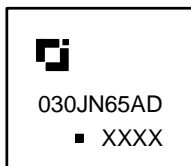
FEATURE

- 600V Breakdown Voltage
- Ultra Low $R_{DS(ON)} = 30m\Omega @ V_{GS} = 10V$
- New Technology in High Voltage Device
- Ultra Low Gate Charge
- 100% Avalanche Tested

APPLICATIONS

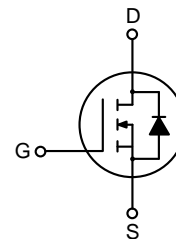
- EV Charger
- Power Factor Correction (PFC)
- Solar Power
- Power Storage

MARKING



030JN65AD =Device code.
 Solid dot =Green molding compound device,
 if none, the normal device
 XXXX =Code

EQUIVALENT CIRCUIT



Order Code	Package	Marking	Parking
CJWT030JN65AD	TO-247	030JN65AD	Tube

Absolute Maximum Ratings (T_C=25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V _{DSS}	Drain-Source Voltage	600	V
V _{GSS}	Gate-Source Voltage	±20	V
	Gate-Source transient voltage, AC (f >1Hz)	±30	
I _D	Drain Current	80	A
	Drain Current @T _C =100°C	50	
I _{DM}	Pulsed Drain Current, tp limited by T _{J,MAX}	240	A
E _{AS}	Avalanche Energy, Single Pulse ⁽¹⁾	2500	mJ
I _S	Continuous Diode Forward Current	80	A
I _{S,PULSE}	Diode Pulsed Current, limited by T _{J,MAX}	240	A
dv/dt	MOSFET dv/dt Ruggedness, V _{DS} ≤480V	50	V/nS
	Reverse Diode dv/dt, V _{DS} ≤480V, I _{SD} ≤I _D	50	
P _D	Power Dissipation @T _C =25°C	481	W
T _J , T _{STG}	Junction and Storage Temperature Range	-55 to 150	°C

(1) V_{DD} = 100V, R_G = 25Ω, L=60mH, Starting T_J= 25°C.

Thermal Characteristics

Symbol	Parameter	Value	Unit
R _{θJC}	Thermal resistance, Maximum Junction-to-Case	0.26	°C/W
R _{θJA}	Thermal resistance, Maximum Junction-to-Ambient	62	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Ration			Unit
			Min.	Typ.	Max.	
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	600			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{GS} =0V, V _{DS} =600V			100	μA
I _{GSS}	Gate-Source leakage current	V _{GS} =±20V			±200	nA
		V _{GS} =±30V			±500	nA
V _{GS(th)}	Gate-Source Threshold Voltage	I _D =2.2mA, V _{DS} =V _{GS}	3		5	V
R _{DS(on)}	Static Drain-Source On-Resistance	I _D =35A, V _{GS} =10V		26	30	mΩ
V _{SD}	Drain-Source Diode Forward Voltage	I _{SD} =35A, T _c =25°C			1.5	V
DYNAMIC PARAMETERS						
C _{ISS}	Input Capacitance	V _{DS} =50V, V _{GS} =0V f=100KHz		8473		pF
C _{OSS}	Output Capacitance			457		
C _{RSS}	Reverse Transfer Capacitance			13		
C _{O(er)}	Effective output capacitance, energy Related ⁽²⁾	V _{GS} =0V, V _{DS} =0...400V		300		pF
C _{O(tr)}	Effective output capacitance, time Related ⁽³⁾			1850		pF
R _g	Gate resistance	Open Drain, f=1MHz		2.4		Ω
SWITCHING PARAMETERS						
t _{d(on)}	Turn-On Delay Time	V _{DD} =400V, I _D =40A R _G =2Ω, V _{GS} =10V, T _J =25°C		39		ns
t _r	Current Rise Time			40		
t _{d(off)}	Turn-Off Delay Time			148.8		
t _f	Current Fall Time			4.2		
Gate Charge Characteristics						
Q _{gs}	Gate to source charge	V _{DD} =400V, I _D =40A V _{GS} =0 to 10V		56.7		nC
Q _{gd}	Gate to drain charge			115.1		
Q _g	Gate charge total			226.2		
Reverse Diode Characteristics						
t _{rr}	Reverse recovery time	V _R =400V, I _F =30A di _F /dt=100A/us		175		nS
Q _{rr}	Reverse recovery charge			1.3		μC
I _{rrm}	Peak reverse recovery current			13.9		A

(2) C_{O(er)} is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400V.

(3) C_{O(tr)} is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400V.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

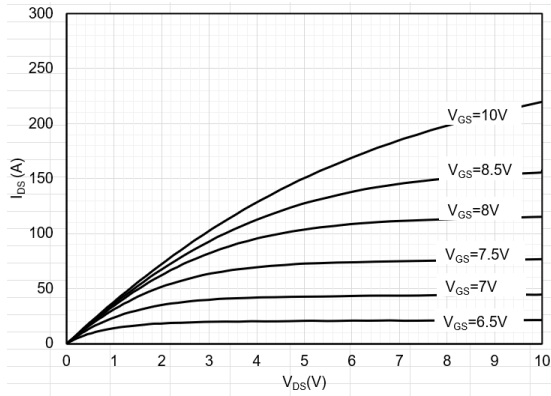


Figure 1: Output Characteristic
($T_J=25^\circ\text{C}$)

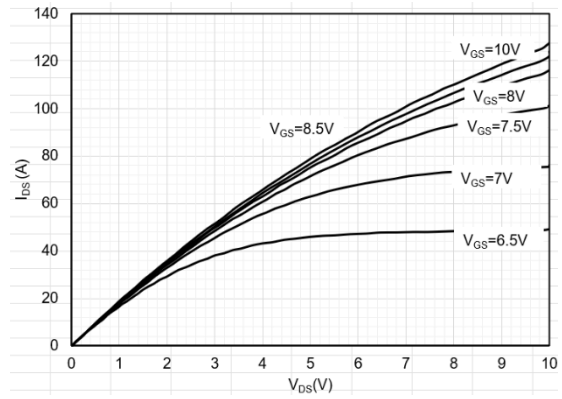


Figure 2: Output Characteristic
($T_J=125^\circ\text{C}$)

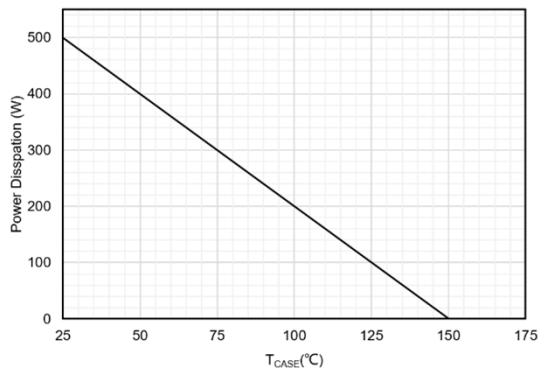


Figure 3: Power Dissipation

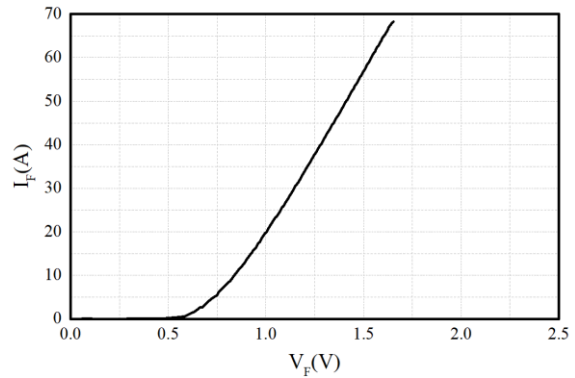


Figure 4: Diode Characteristic
($T_J=25^\circ\text{C}$)

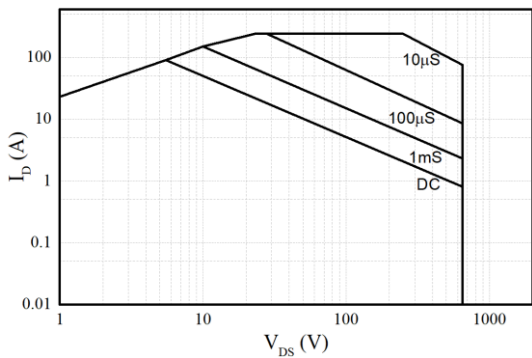


Figure 5: Safe Operating Area
($T_C=25^\circ\text{C}$, $V_{GS}\geq 8\text{V}$)

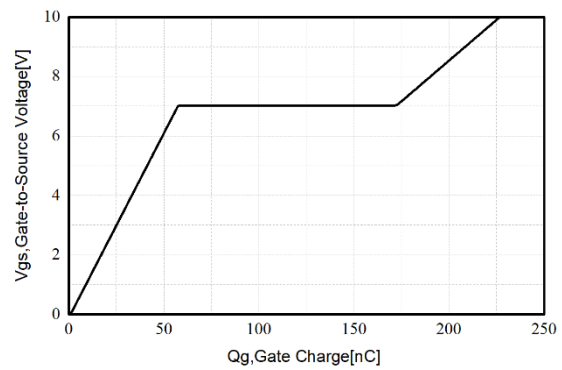


Figure 6: Typ. Gate charge
($V_D=400\text{V}$, $I_D=40\text{A}$)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

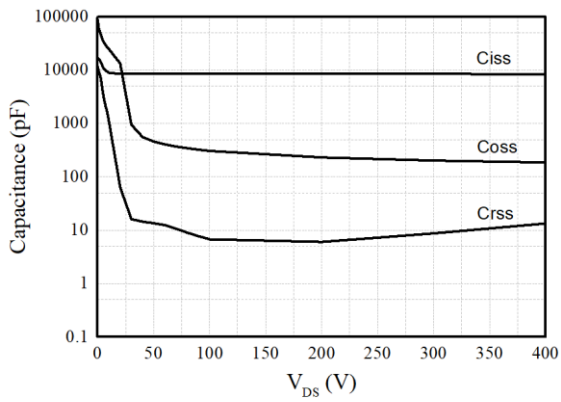


Figure 7: Typ. Capacitances

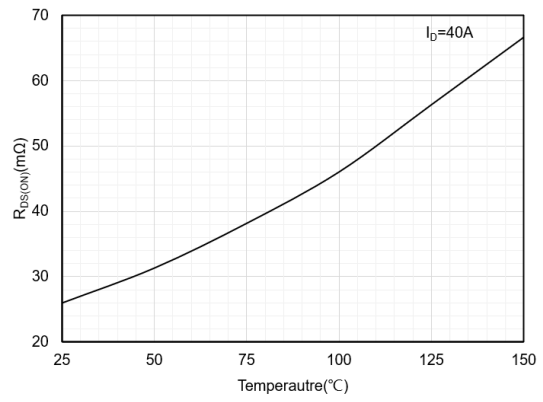


Figure 8: Drain-source on-state resistance

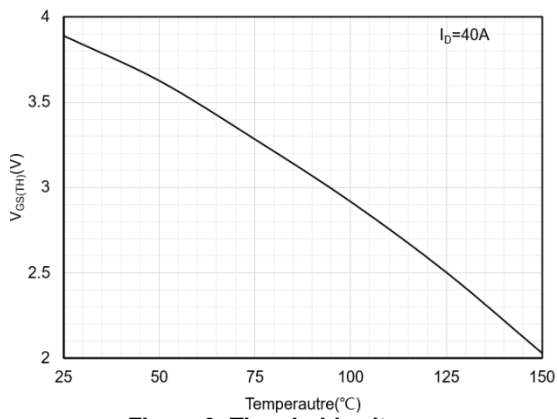


Figure 9: Threshold voltage

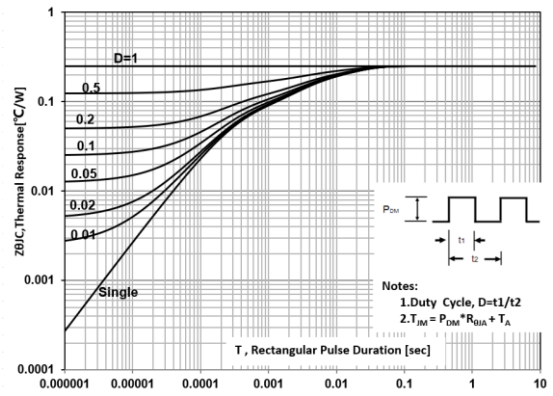


Figure 10: Max. transient thermal impedance

TEST CIRCUIT AND WAVEFORMS



Figure 1: Gate Charge test circuit & waveform

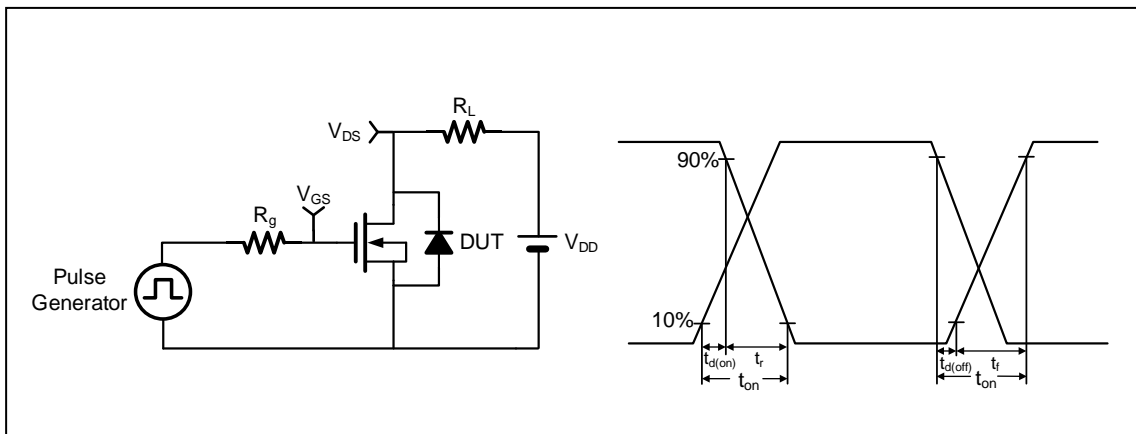


Figure 2: Resistive load switching time test circuit & waveforms

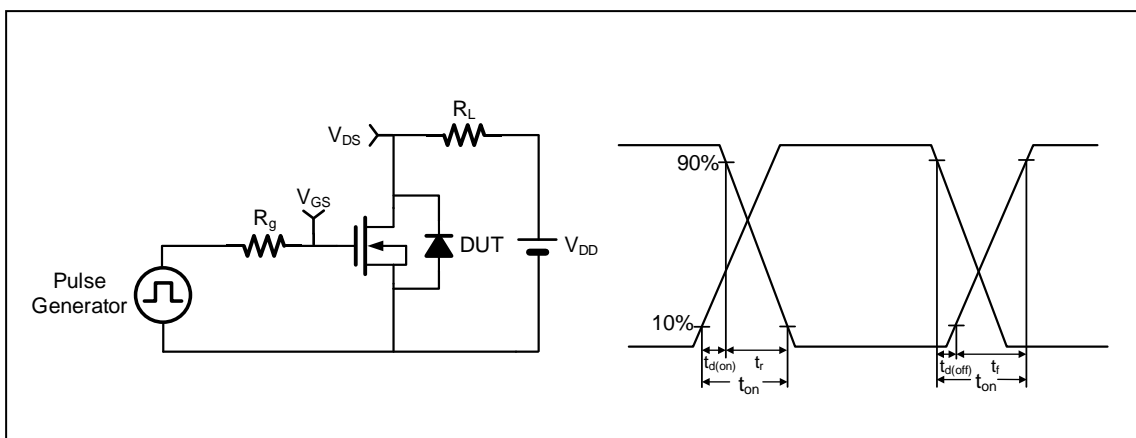
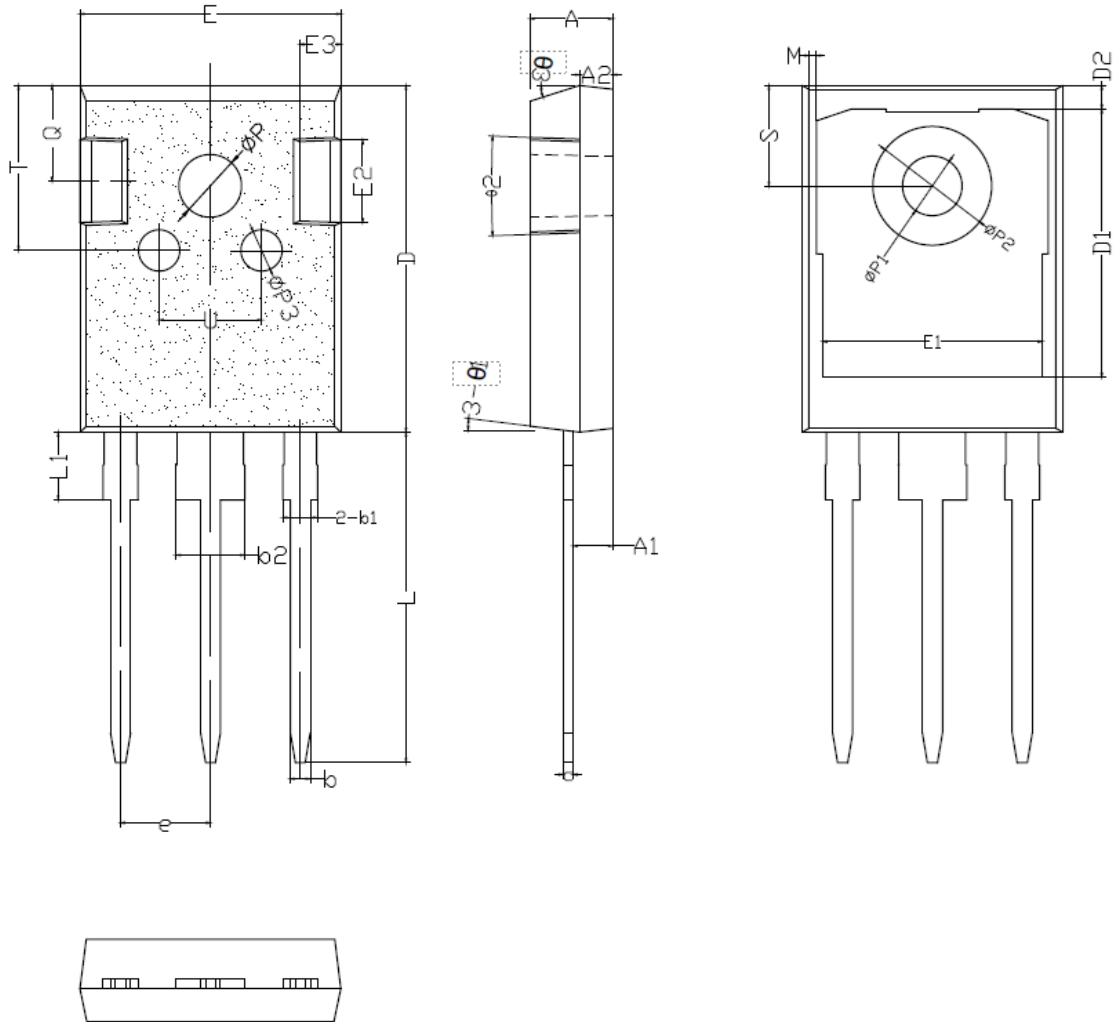


Figure 3: Un-clamped inductive switching (UIS) test circuit & waveforms

TO-247 PACKAGE OUTLINE DIMENSIONS



SYMBOL	mm		
	MIN	NOM	MAX
*A	4.90	5.00	5.10
*A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
*b	1.15	1.20	1.25
*b1	1.95	2.10	2.25
*b2	2.95	3.10	3.25
*c	0.55	0.60	0.65
*D	20.90	21.00	21.10
D1	16.35	16.55	16.75
D2	1.05	1.20	1.35

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*E	15.70	15.80	15.90
E1	13.10	13.25	13.40
E2	4.85	4.95	5.10
E3	2.40	2.50	2.60
*e	5.40	5.44	5.48
*L	19.80	19.98	20.15
*L1	-	-	4.30
*ΦP	3.40	3.50	3.60
*ΦP1	6.90	7.10	7.30
ΦP2	2.40	2.50	2.60
ΦP3	2.40	2.50	2.60
Q	5.60	5.80	6.00
*S	6.05	6.15	6.25
T	9.80	10.00	10.20
U	6.00	6.20	6.40
θ1	5°	7°	9°
θ2	1°	3°	5°
θ3	13°	15°	17°
*为管控尺寸			